

EA40-CX UMA/Muxless Schematics Document Ivy Bridge Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

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UMA C

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Title			
Cover Page			
Size	Document Number	Rev	
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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Leave floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0: connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB	
		Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

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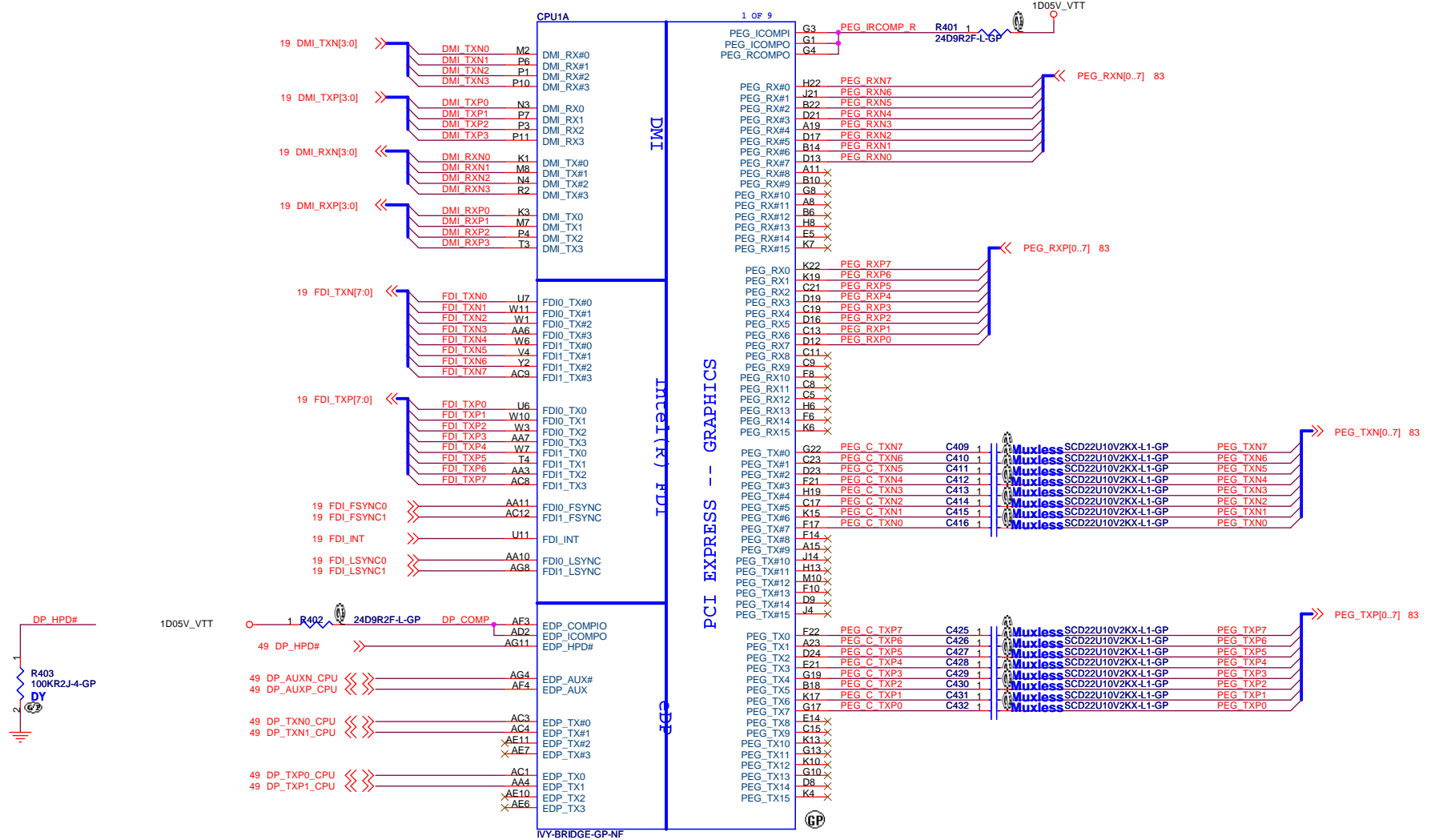
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Table of Content

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SSID = CPU



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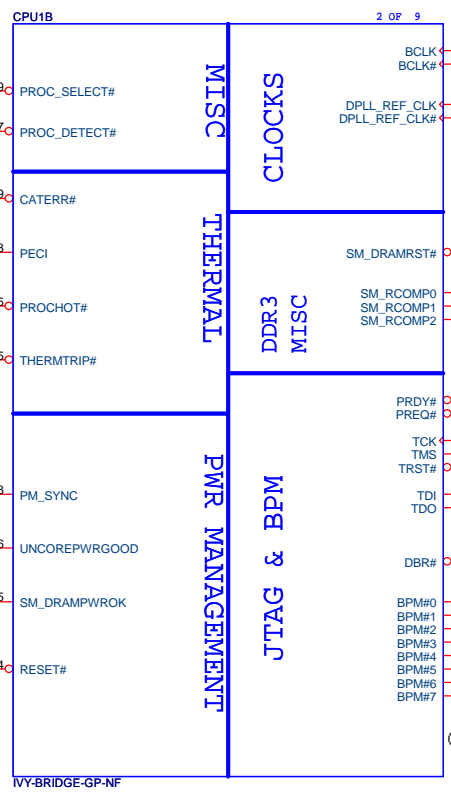
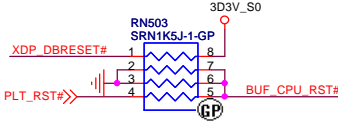
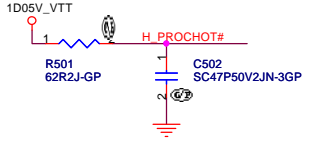
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Title: **CPU (PCIe/DMI/FDI)**

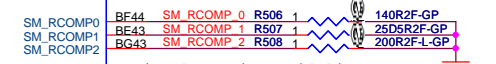
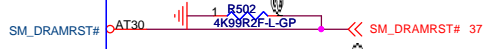
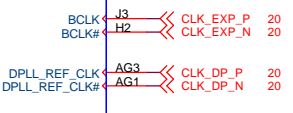
Size A3 Document Number **EA40 CX** Rev **-3**

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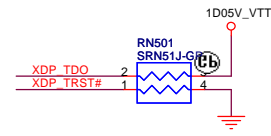
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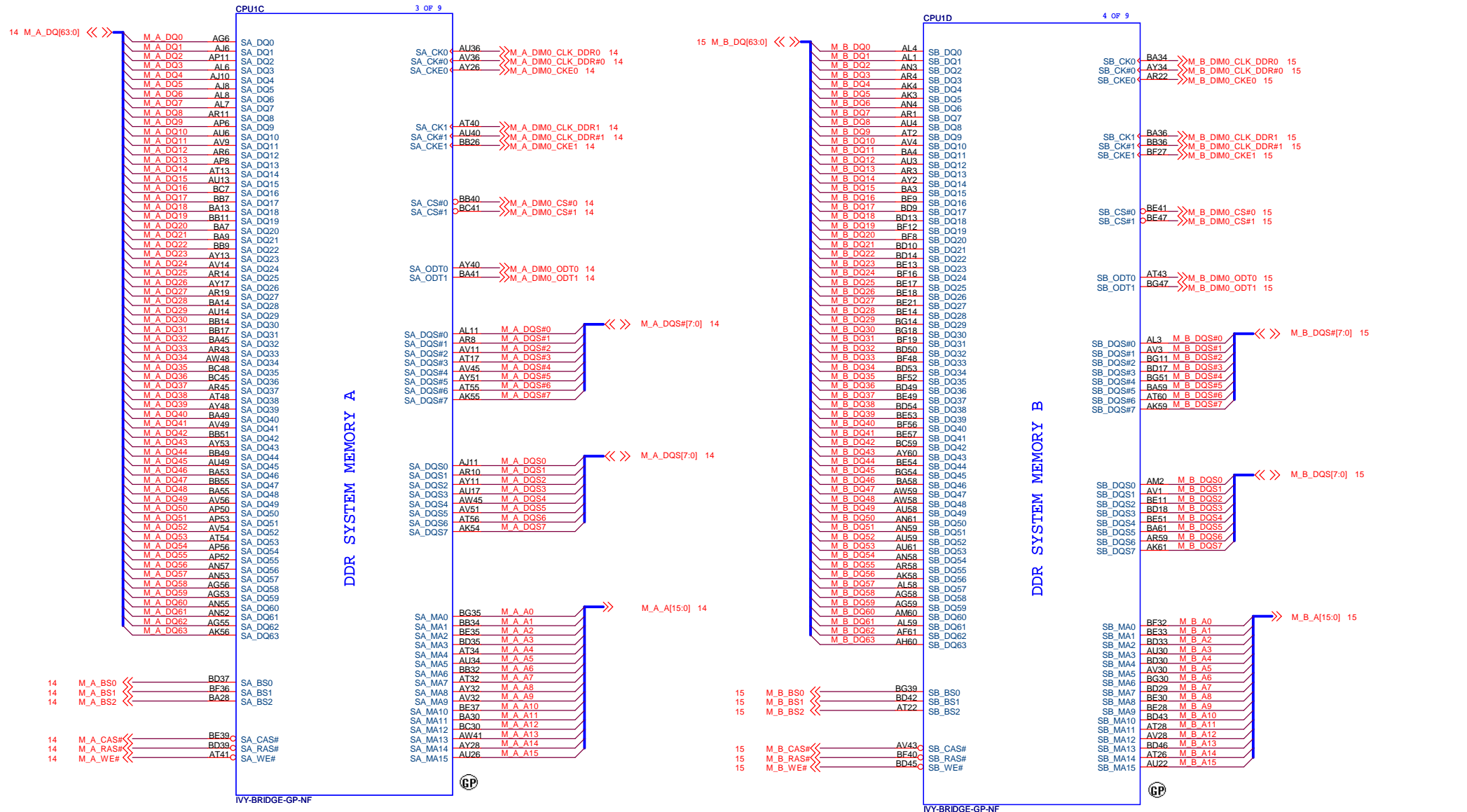
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



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Title CPU (THERMAL/CLOCK/PM)		
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Title: **CPU (DDR)**

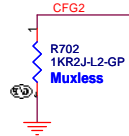
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SSID = CPU

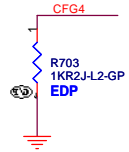
PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed



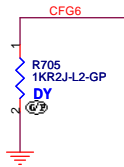
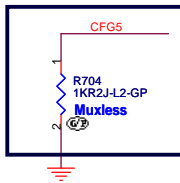
Enabl EDP function

CFG4 1: Disable
0: Enable



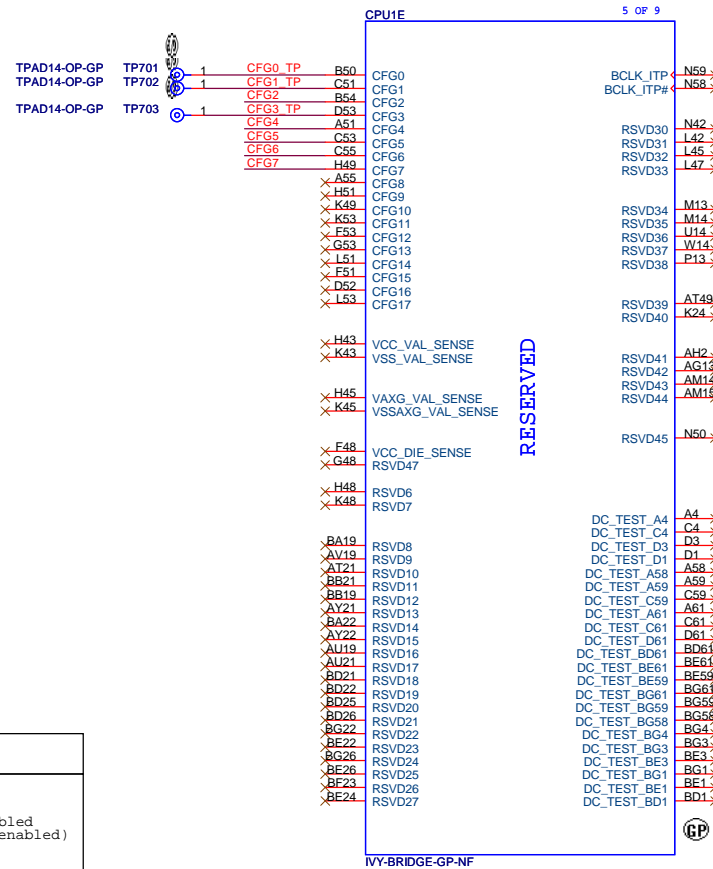
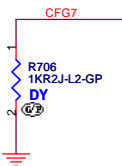
PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING

CFG7 1: PEG Train immediately following xxRESETB de assertion
0: PEG Wait for BIOS for training



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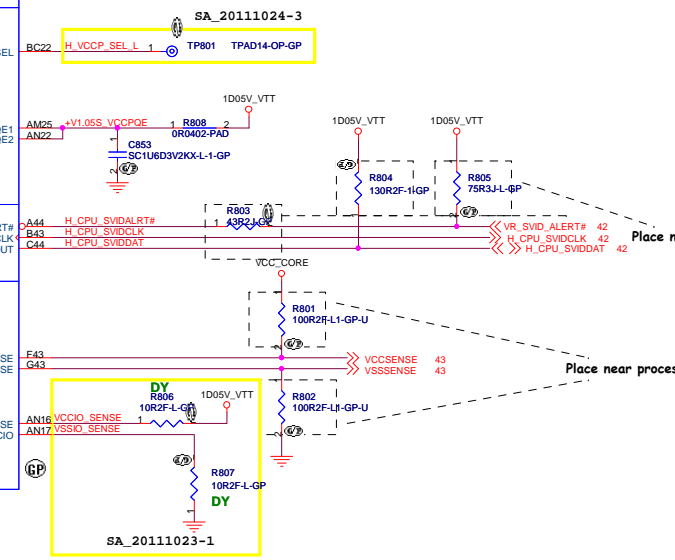
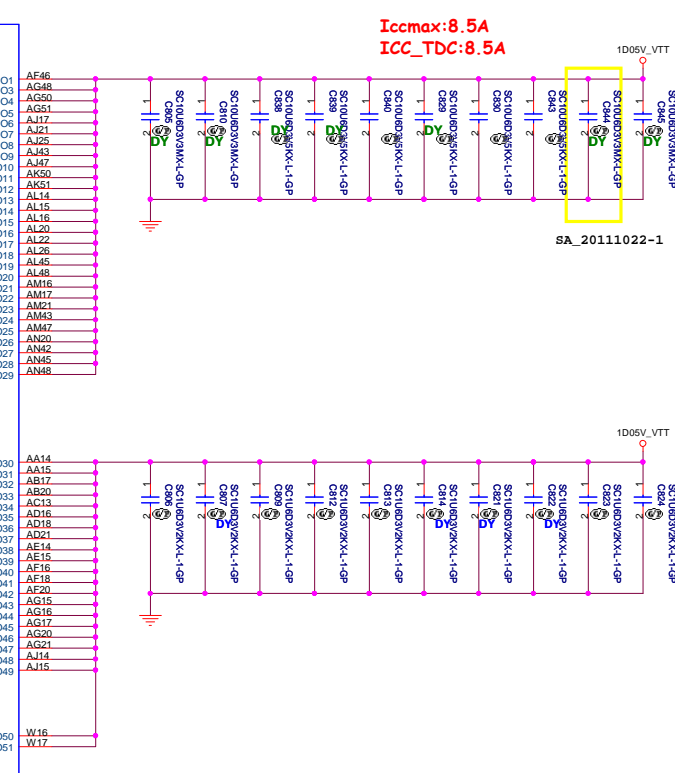
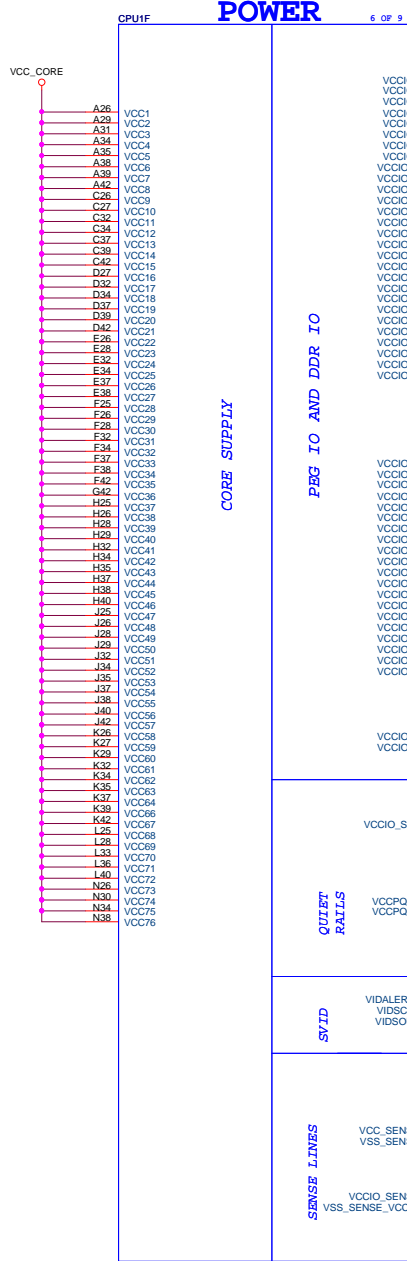
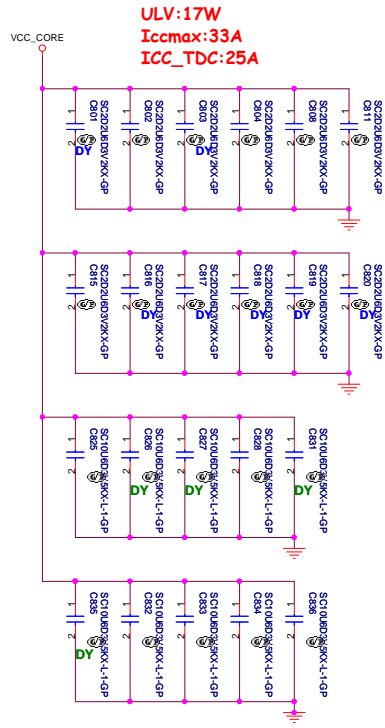
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Title CPU (RESERVED)		
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SSID = CPU

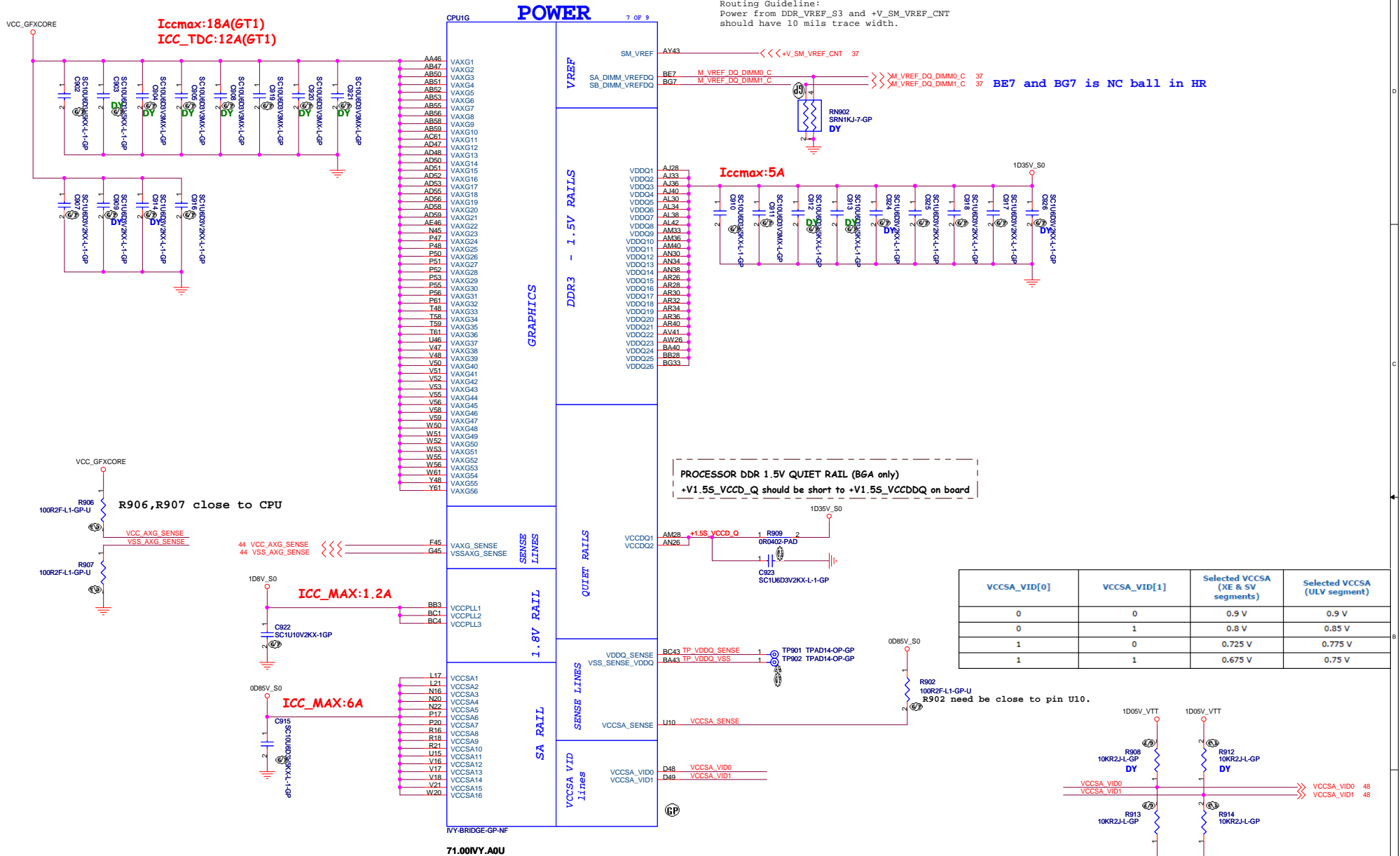


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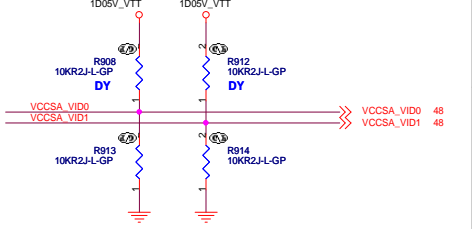
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Title		
CPU (VCC CORE)		
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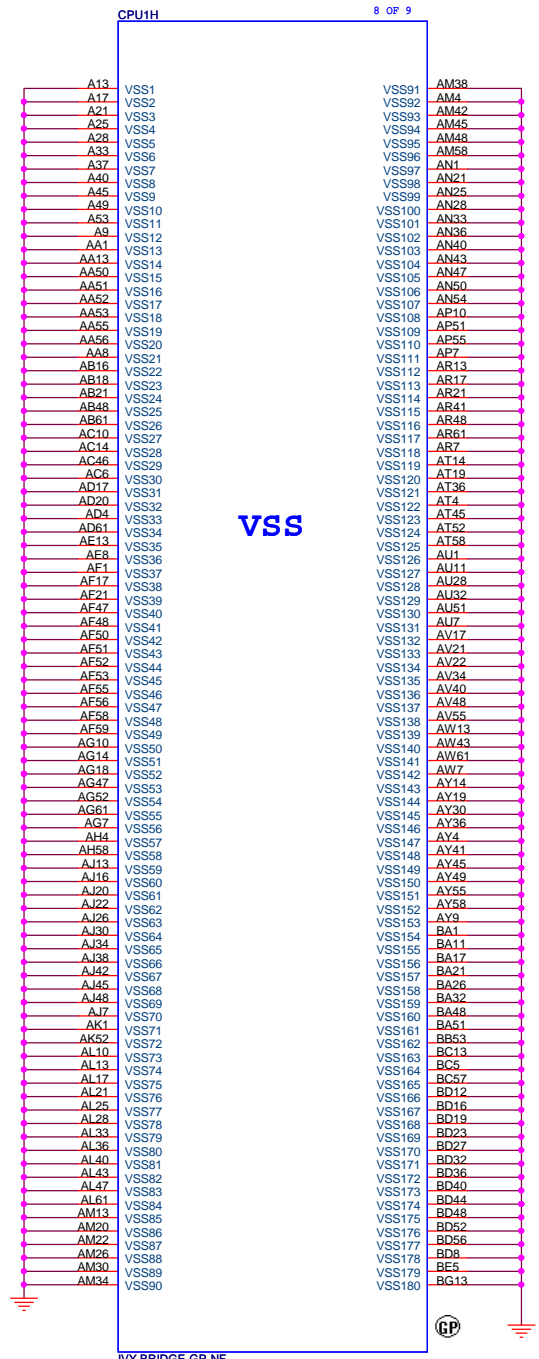
PROCESSOR DDR 1.5V QUIET RAIL (B6A only)
 +V1.5S_VCCD_Q should be short to +V1.5S_VCCDDQ on board

VCCSA_VID[0]	VCCSA_VID[1]	Selected VCCSA (XE & SV segments)	Selected VCCSA (ULV segment)
0	0	0.9 V	0.9 V
0	1	0.8 V	0.85 V
1	0	0.725 V	0.775 V
1	1	0.675 V	0.75 V

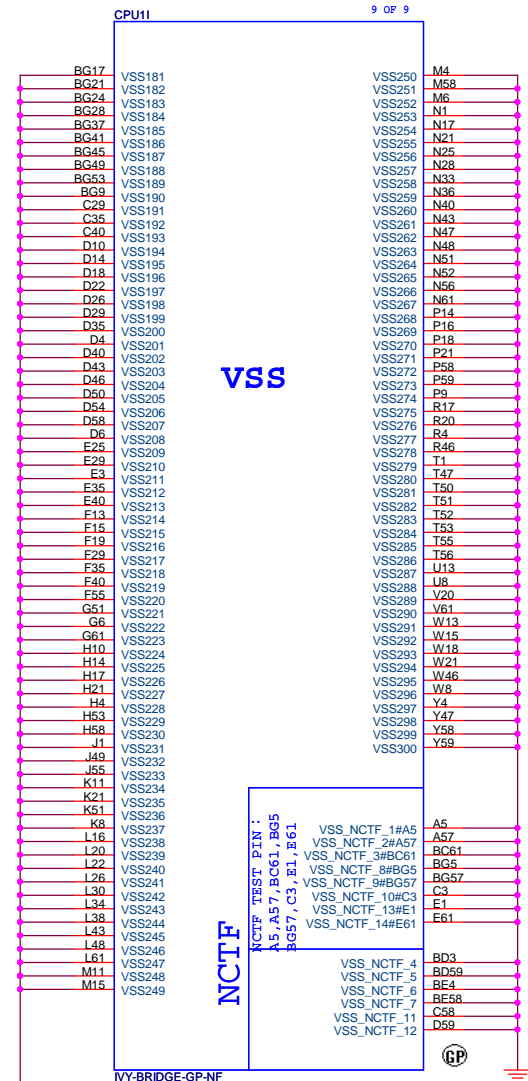


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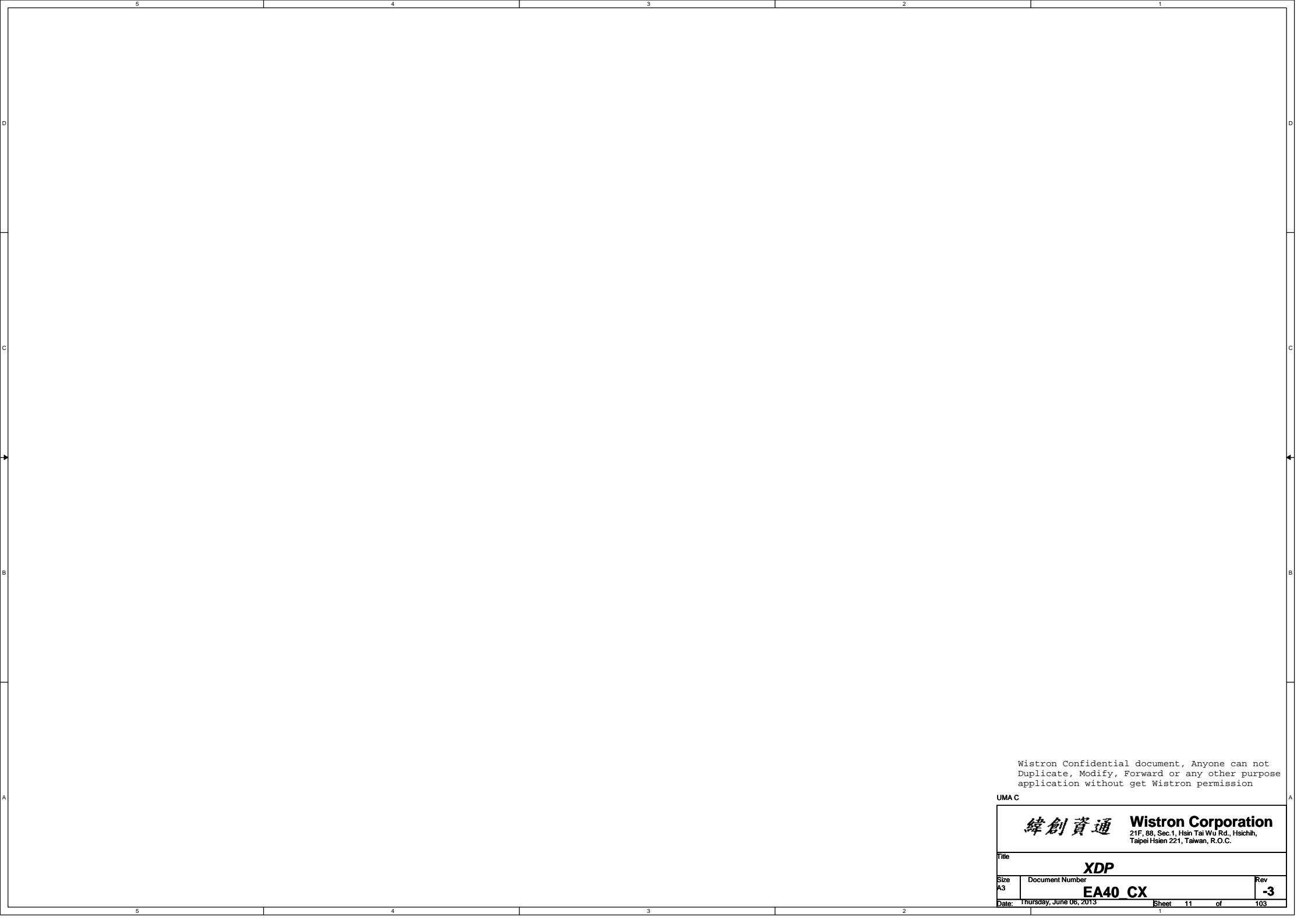
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Title: **CPU (VSS)**

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Title	Reserved	
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B

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Title **Reserved**

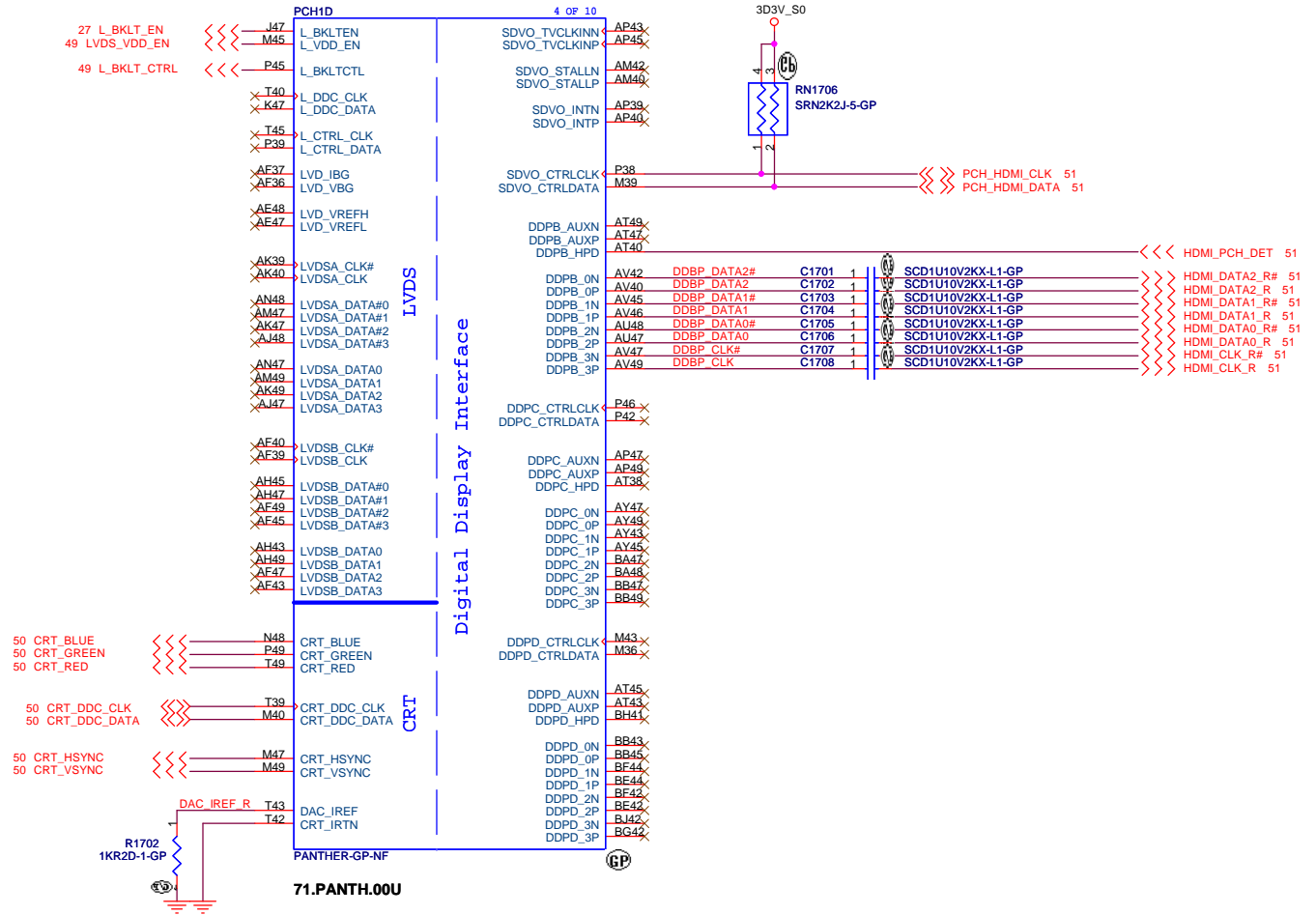
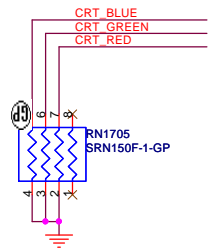
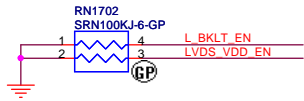
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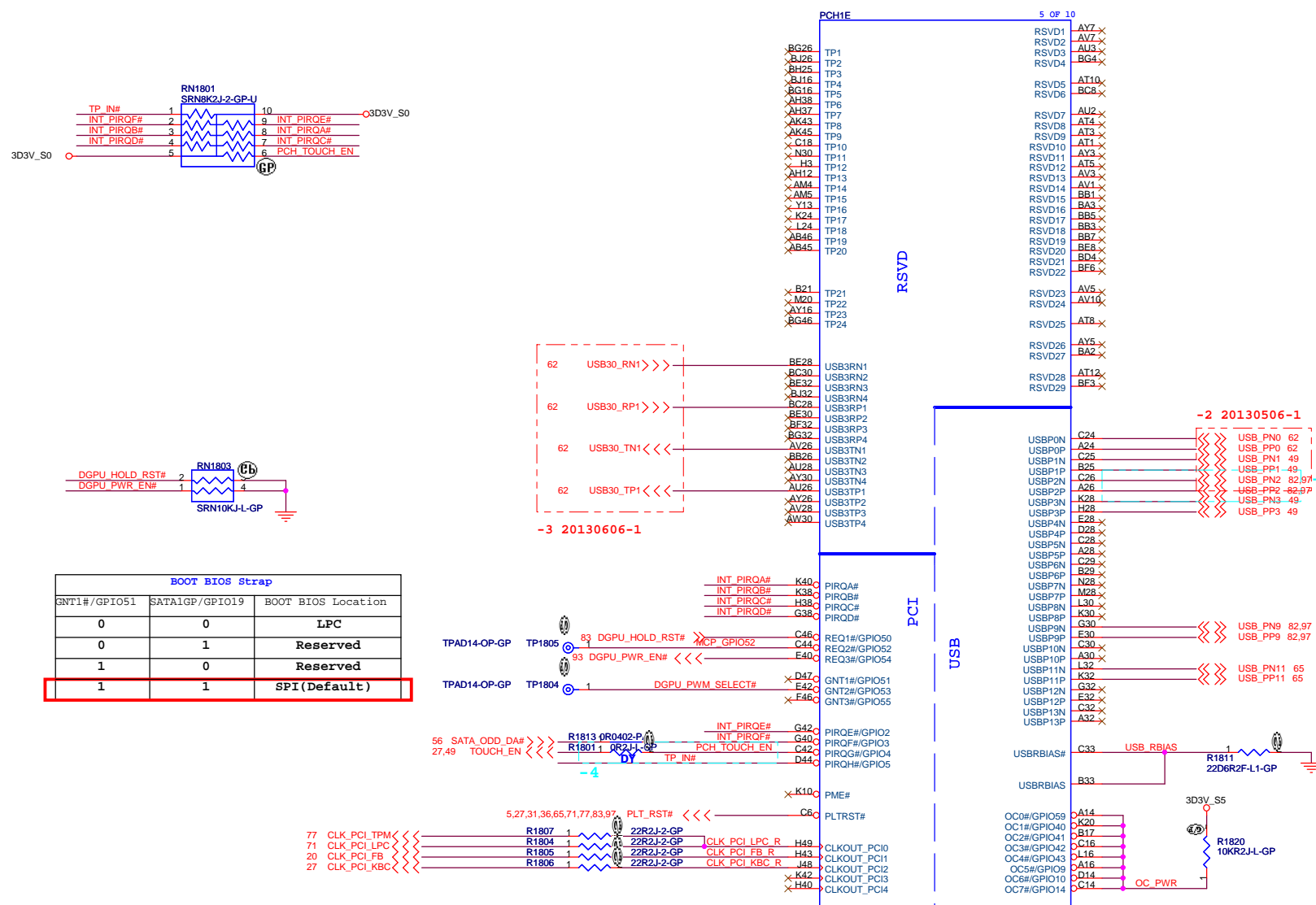
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Title: **PCH (LVDS/CRT/DDI)**

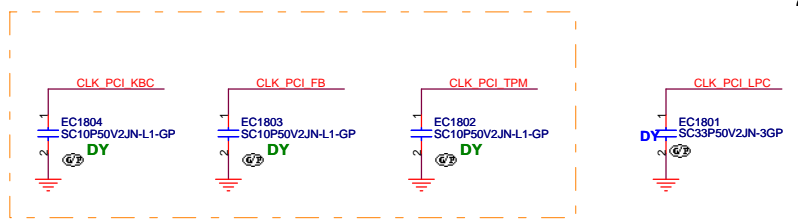
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BOOT BIOS Strap		
GN1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

-1_20130315_EMI



USB Table

Pair	Device
0	USB2.0/USB3.0 Ext. port 1
1	Touch panel -3 20130606-1
2	USB2.0 Ext. port 1
3	CCD
4	
5	
6	may not be available
7	may not be available
8	
9	USB2.0 Ext. port 3
10	
11	Mini Card1 (WLAN+BT)
12	
13	

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Title: **PCH (PCI/USB/NVRAM)**

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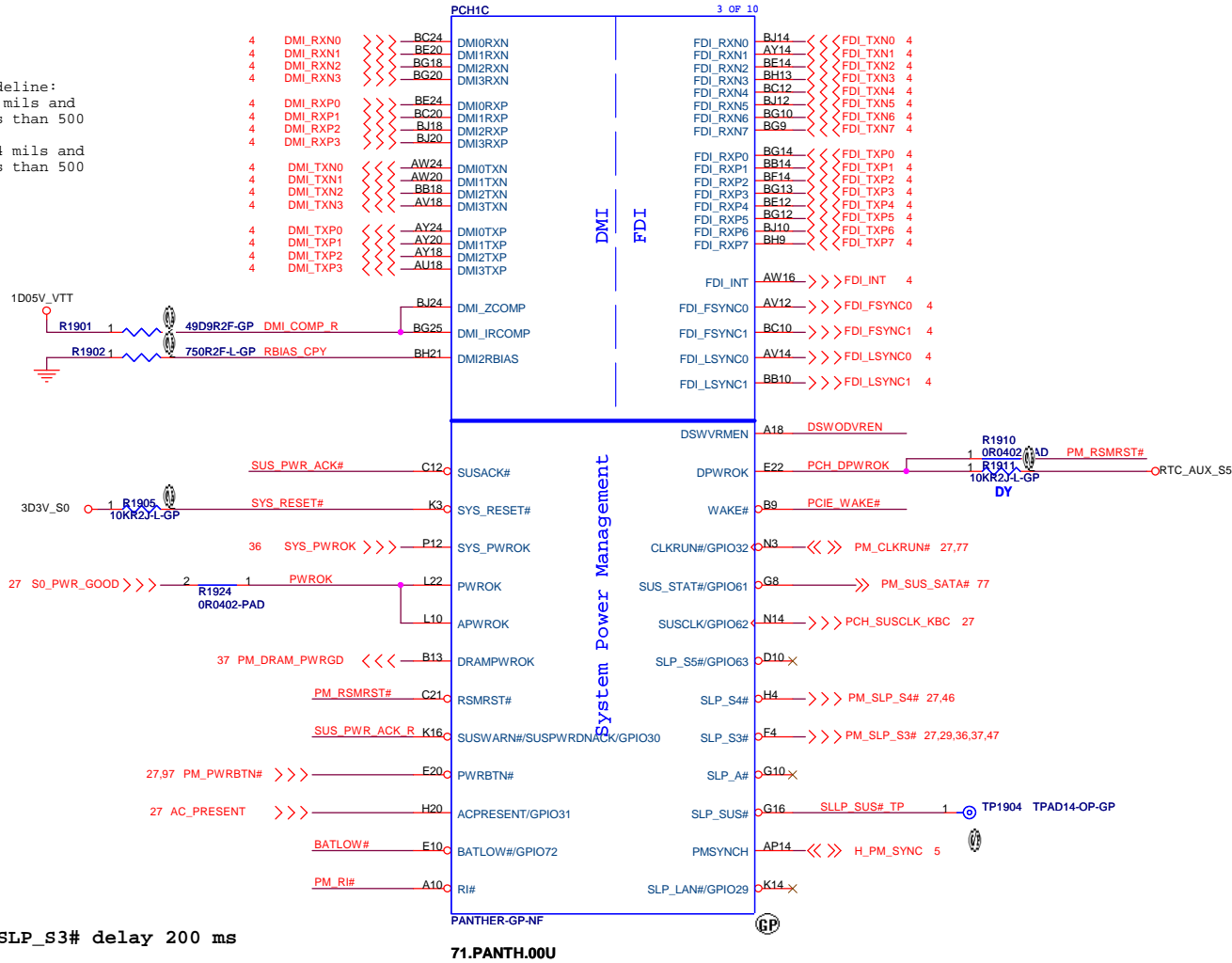
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SSID = PCH

4 DMI_RXN[3:0] <<<< <<<<
 4 DMI_RXP[3:0] <<<< <<<<
 4 DMI_TXN[3:0] <<<< <<<<
 4 DMI_TXP[3:0] <<<< <<<<

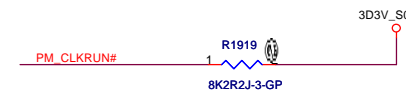
<<<< <<<< FDI_TXN[7:0] 4
 <<<< <<<< FDI_TXP[7:0] 4

Signal Routing Guideline:
 DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
 DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

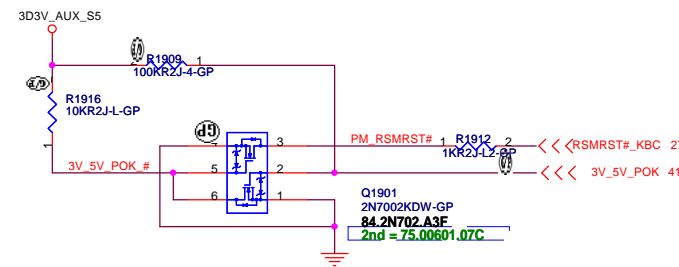
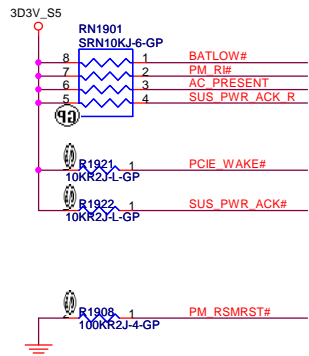


DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

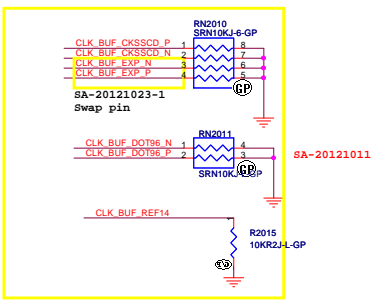
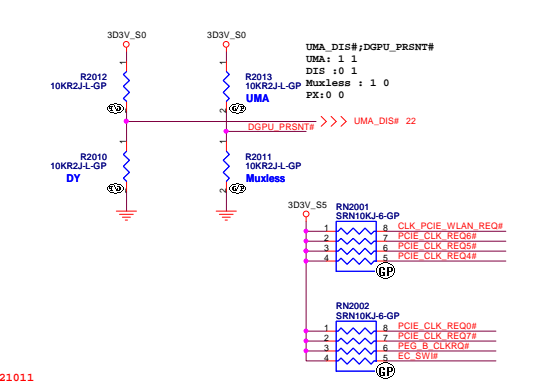
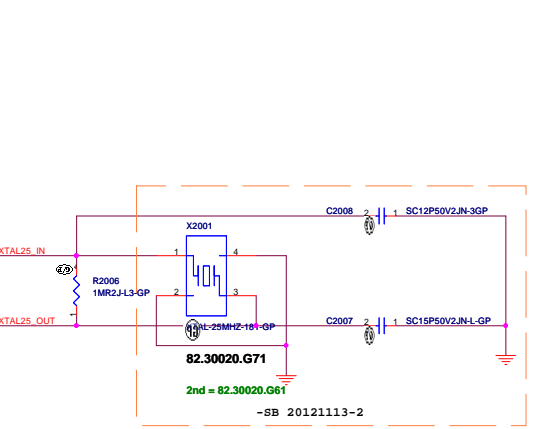
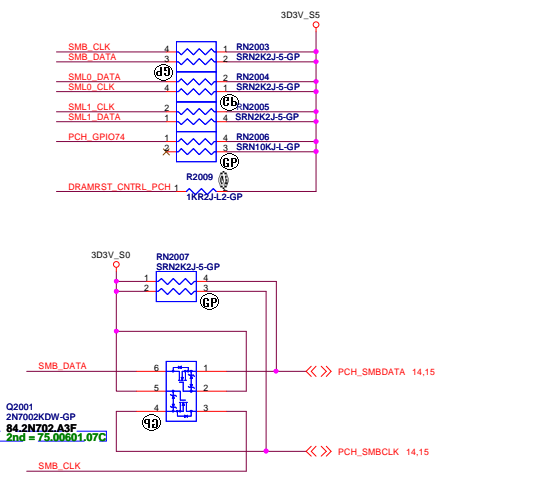
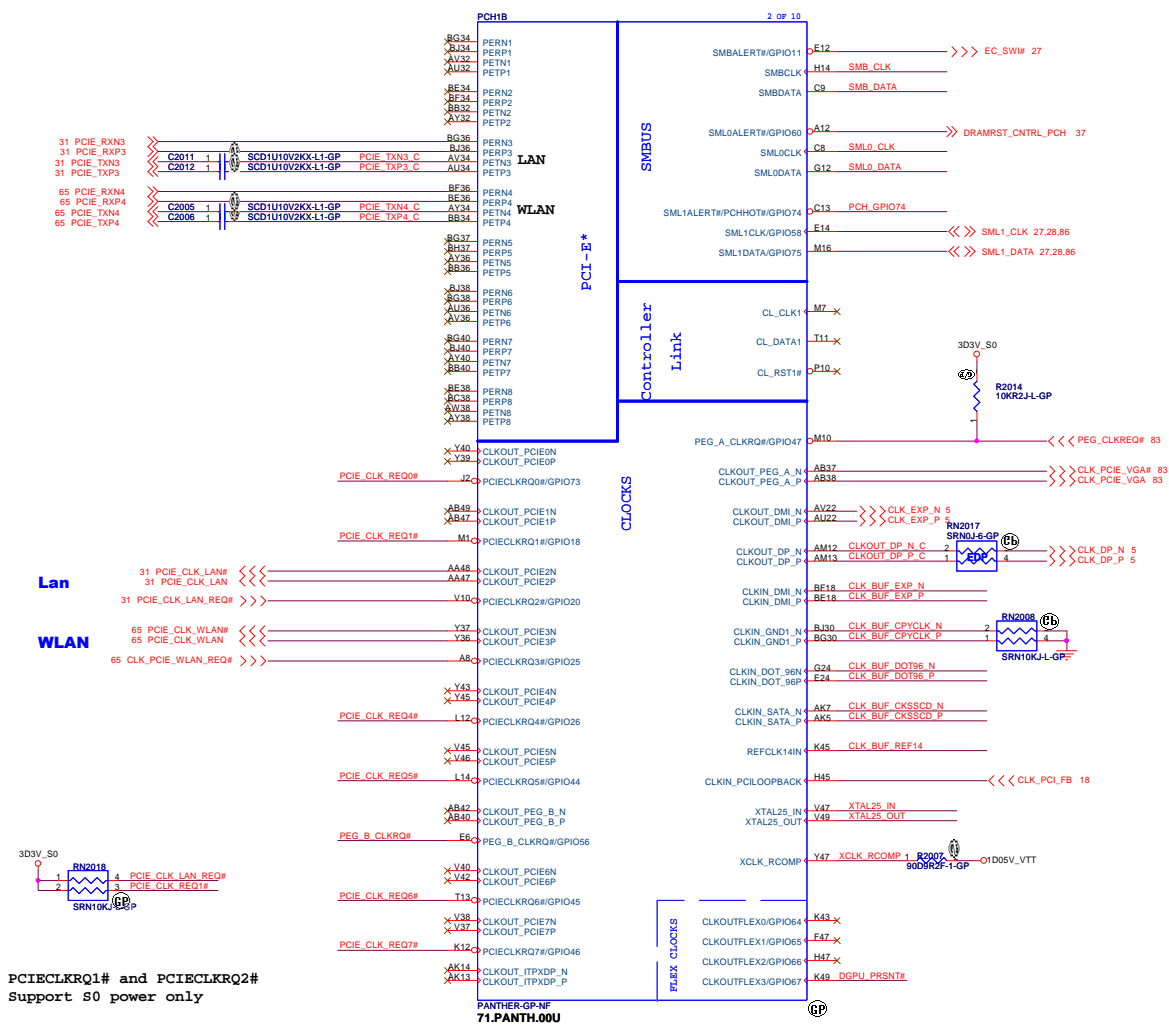


S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



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SSID = PCH



need very close to PCH

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Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size: Document Number

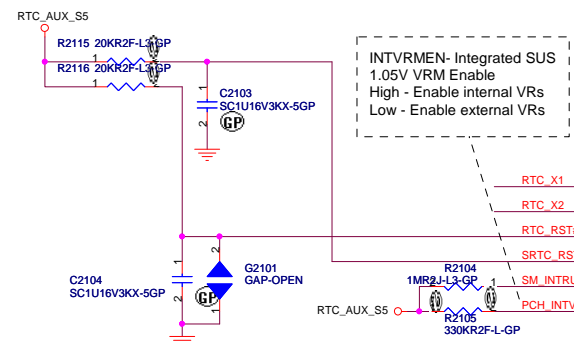
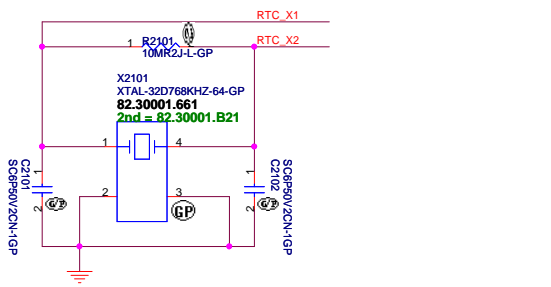
Customer: **EA40 CX**

Date: Thursday, June 20, 2013

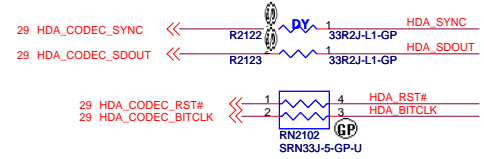
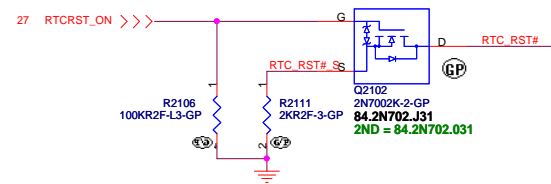
Sheet 20 of 103

Rev: **-3**

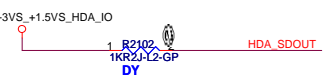
SSID = PCH



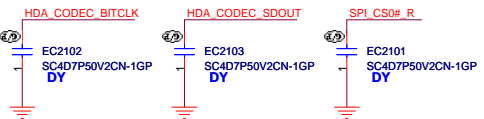
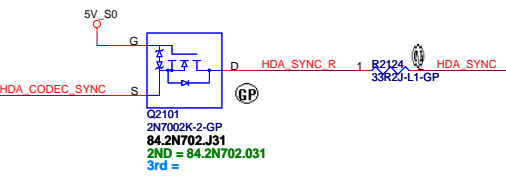
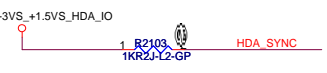
RTC Reset



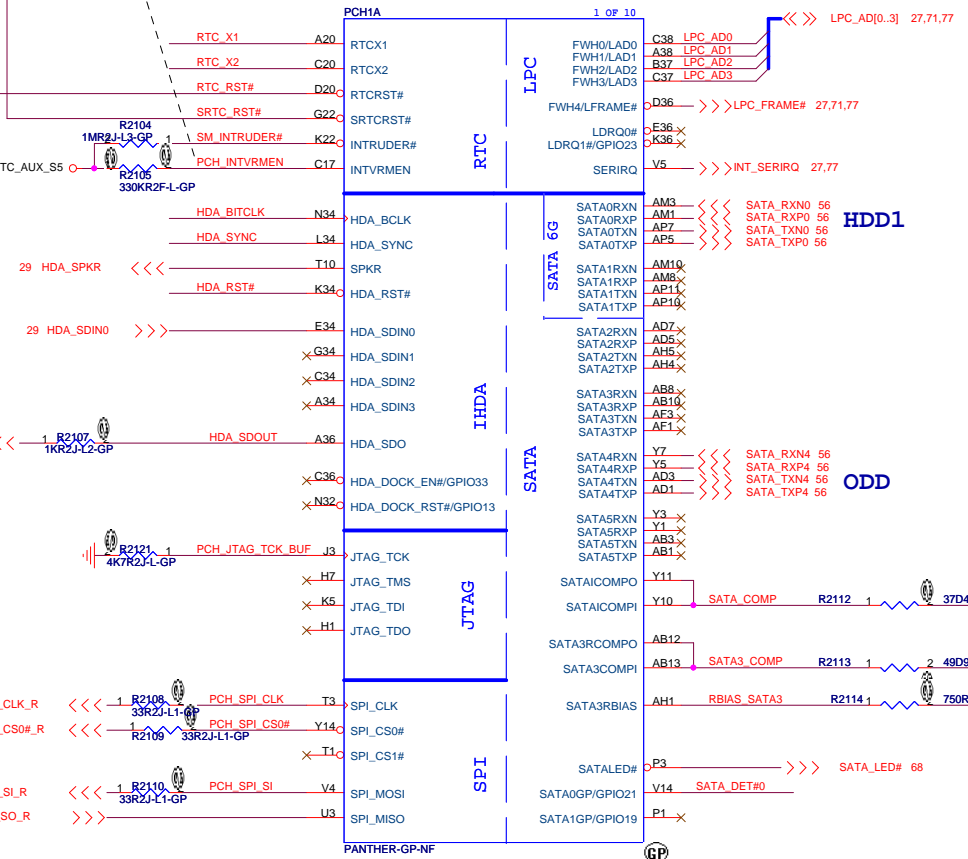
Flash Descriptor Security Override	
HDA_SDOOUT	Low = Default High = Enable



PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



71.PANTH.00U



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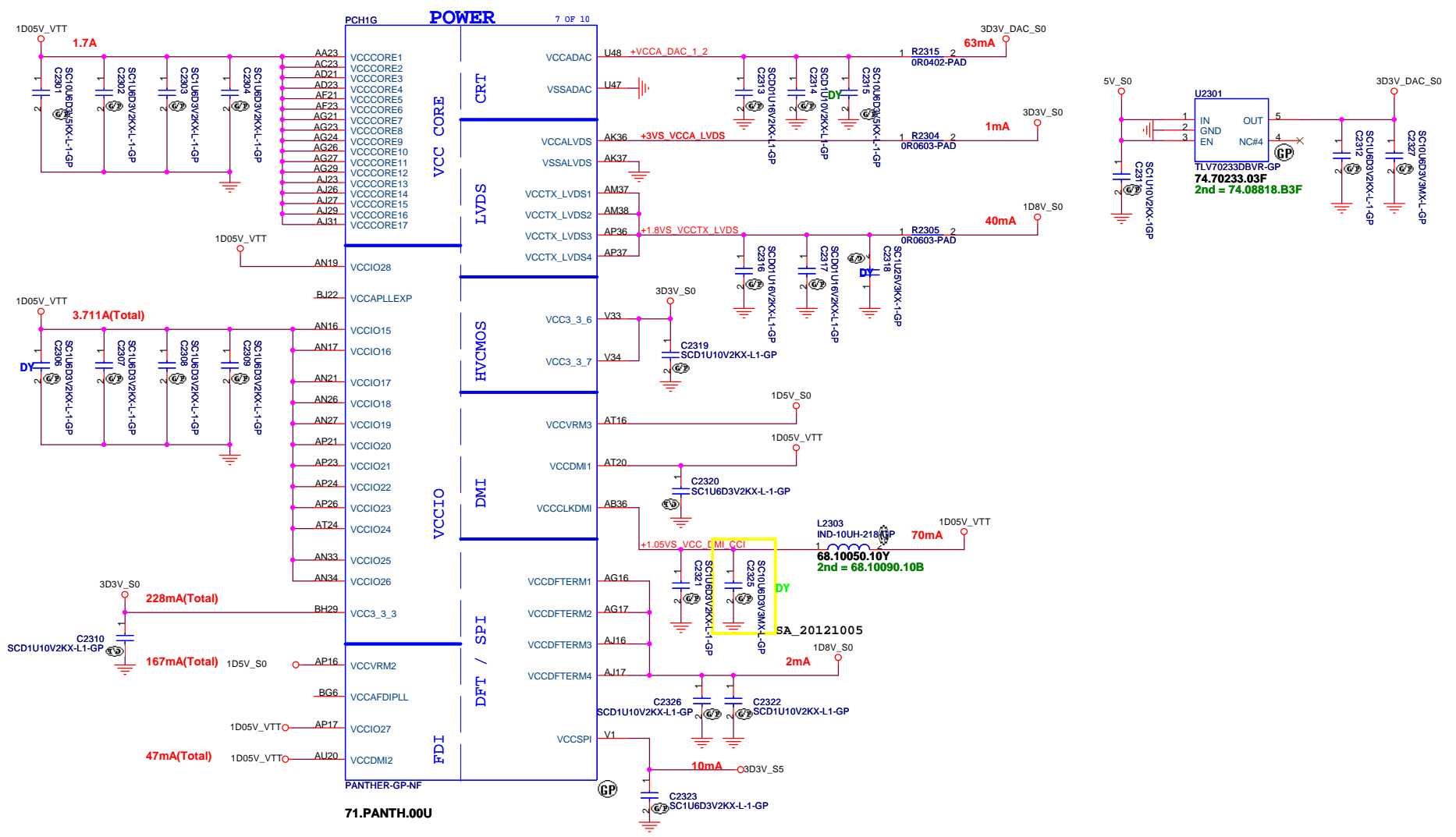
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size: Custom Document Number
Date: Thursday, June 20, 2013

Rev: **-3**

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SSID = PCH



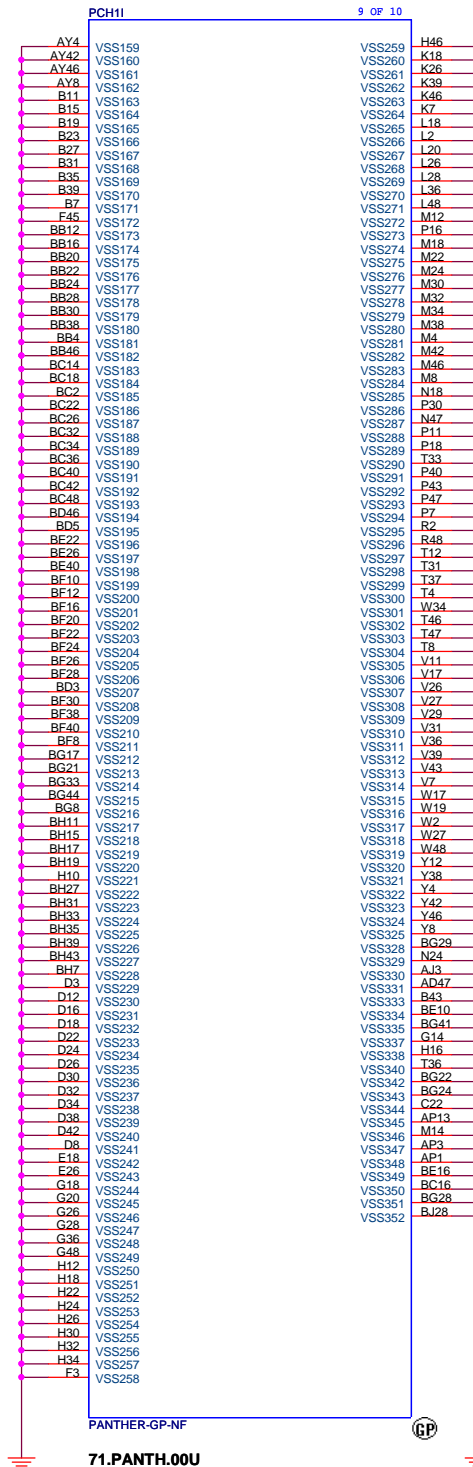
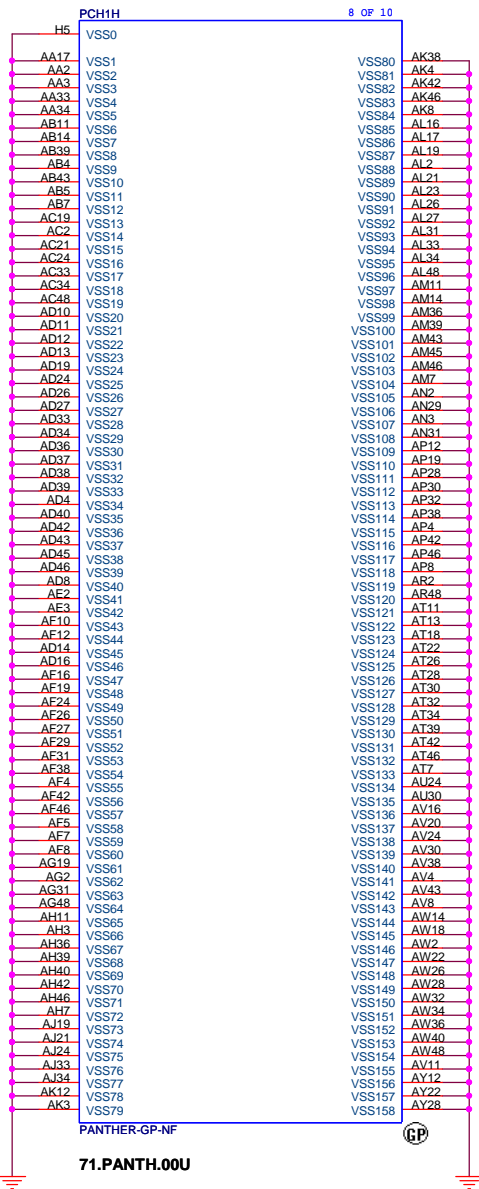
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Title		
PCH (POWER1)		
Size	Document Number	Rev
A3	EA40 CX	-3
Date:	Friday, June 21, 2013	Sheet 23 of 103

SSID = PCH



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Title: **PCH (VSS)**

Size A3 Document Number: **EA40 CX** Rev: **-3**

Date: Thursday, June 06, 2013 Sheet 25 of 103

D

D

C

C

B

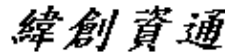
B

A

A

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UMA C

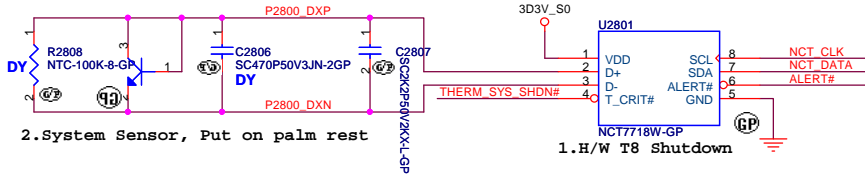
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Clock(colay)</i>	
Size A4	Document Number EA40 CX
Date: Thursday, June 06, 2013	
Rev -3	
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SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Q2801
PMB3904-1-GP
84.03904.L06



2. System Sensor, Put on palm rest

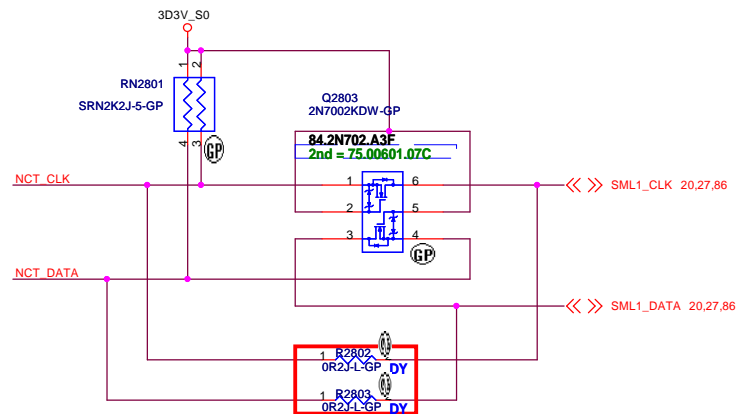
1. H/W T8 Shutdown

ALERT# / T_CRIT#
Pull-up Resistor

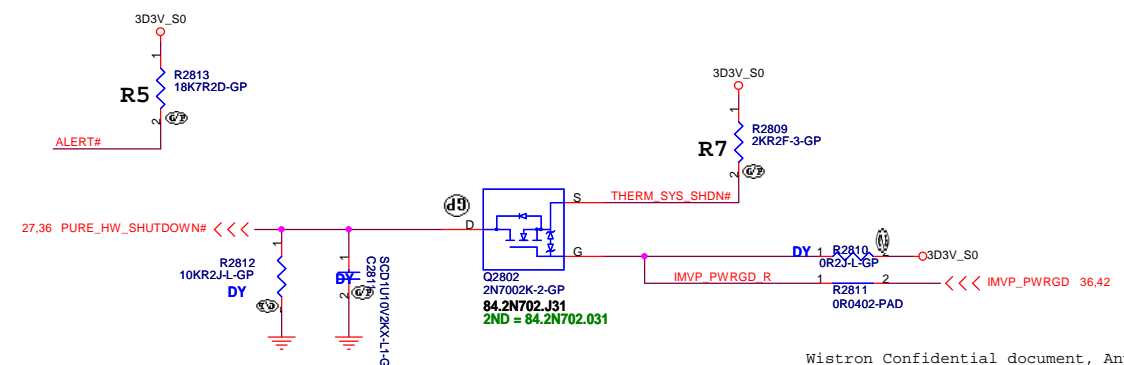
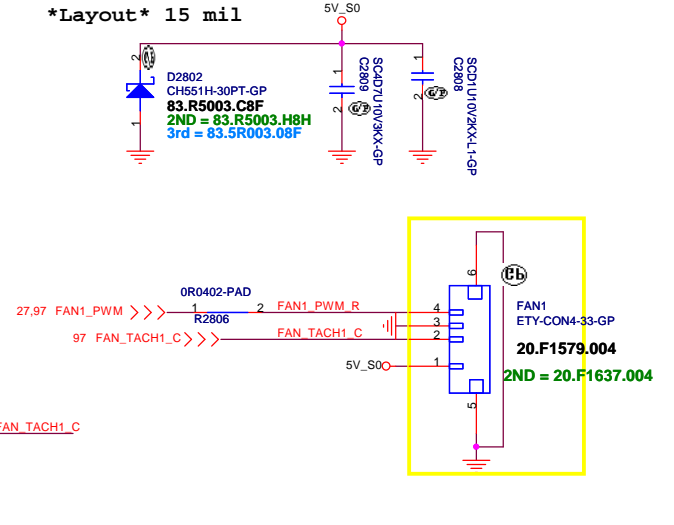
R5	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

SB T8=85 degree



Layout 15 mil



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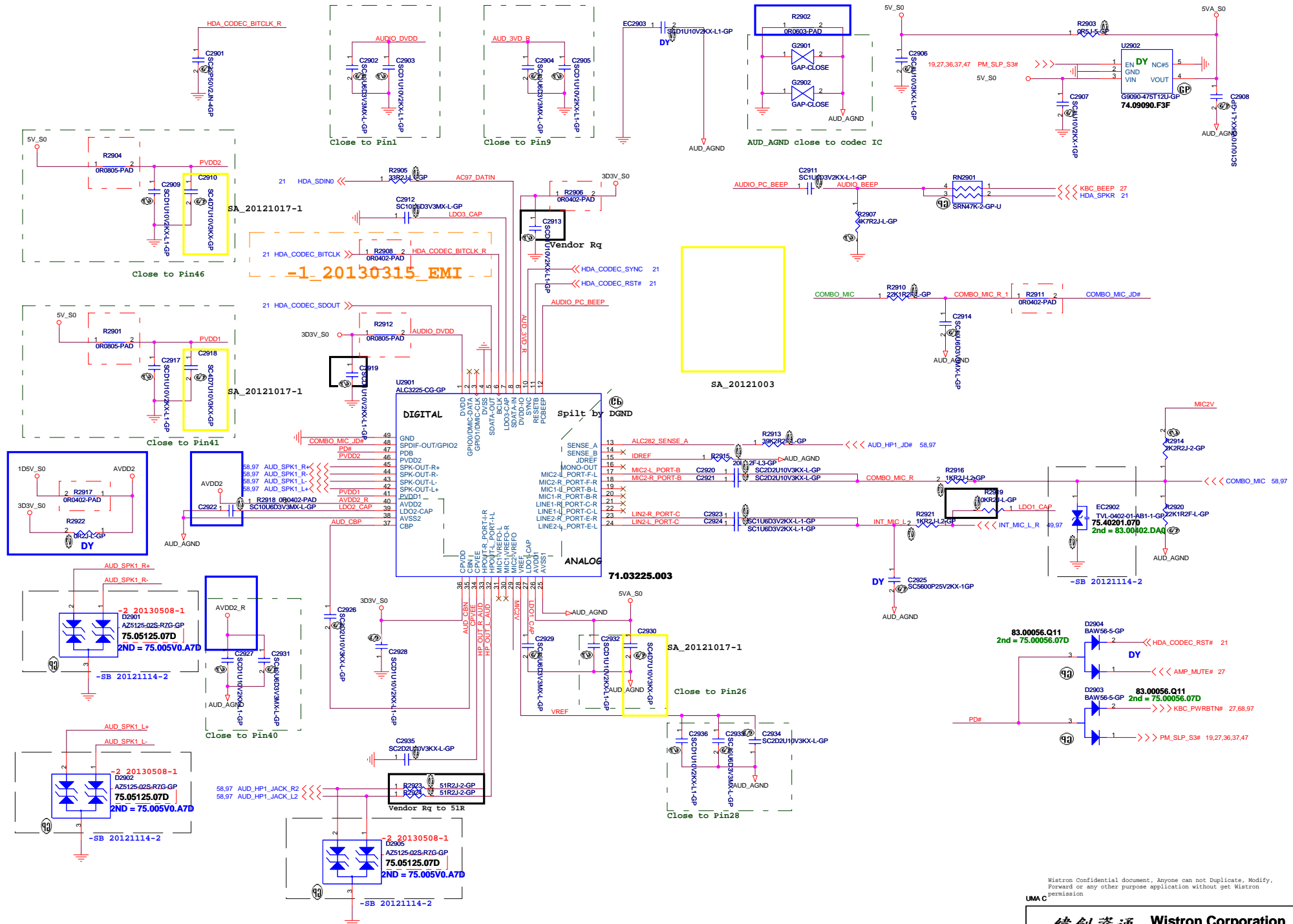
UMA C

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Title: **Thermal NCT7718**

Size	Document Number	Rev
Custom	EA40 CX	-3

Date: Thursday, June 20, 2013 Sheet 28 of 103

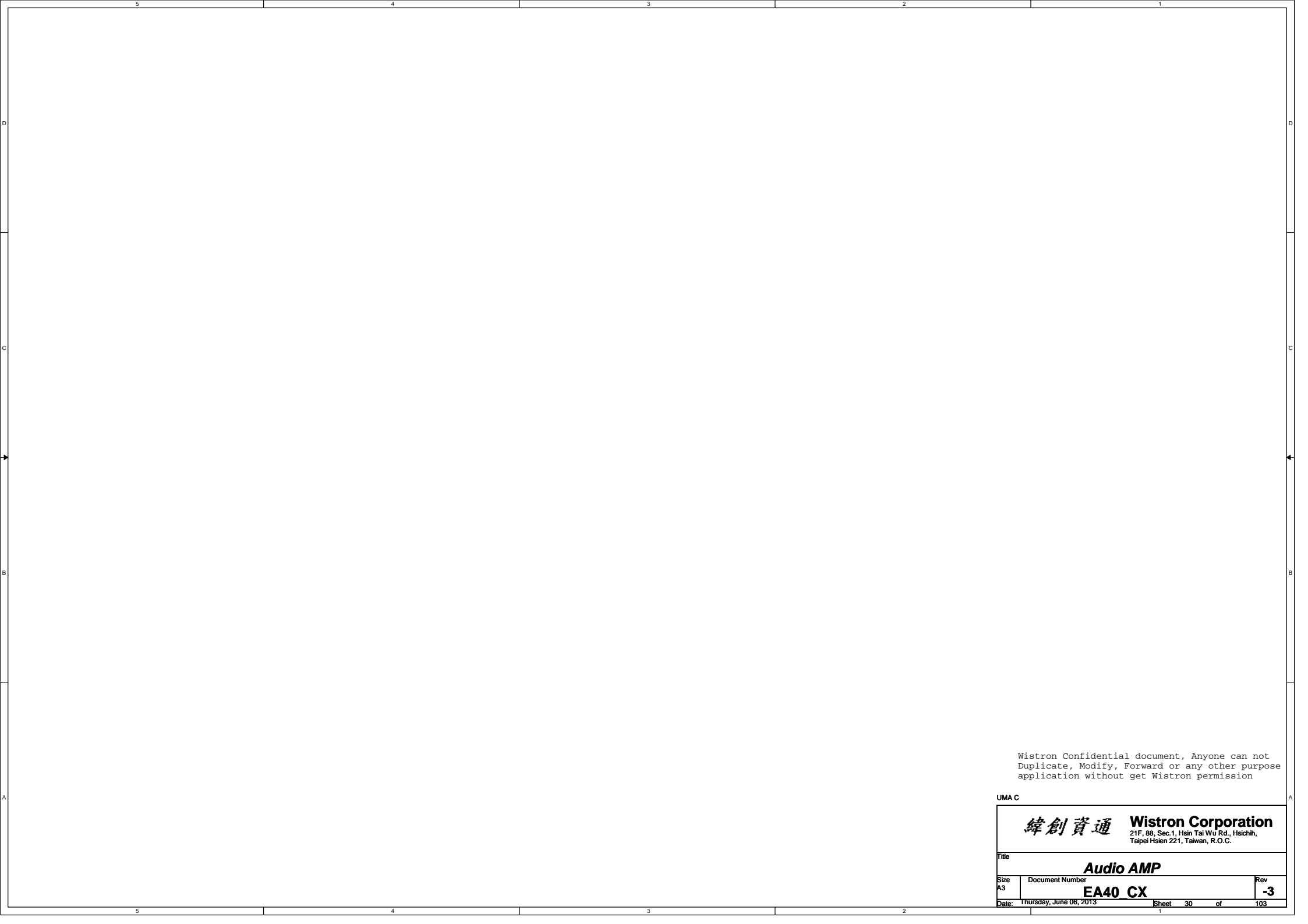


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File		Audio Codec ALC3225	
Size	Document Number	Rev	
Custom	EA40 CX	-3	
Date	Friday, June 21, 2013	Sheet	29 of 103

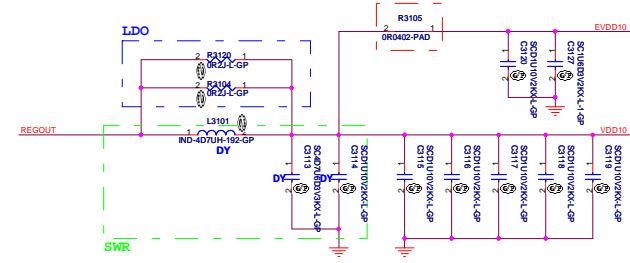
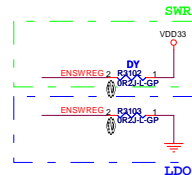
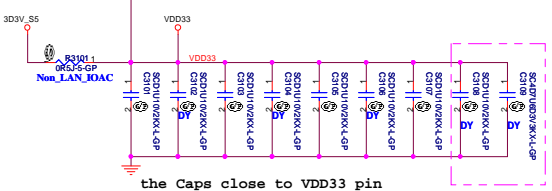
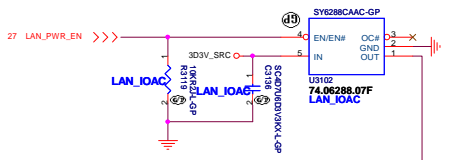


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Taipei Hsien 221, Taiwan, R.O.C.

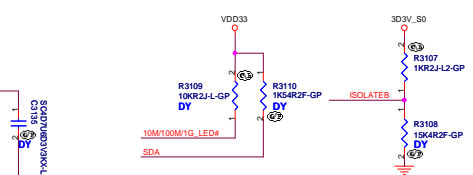
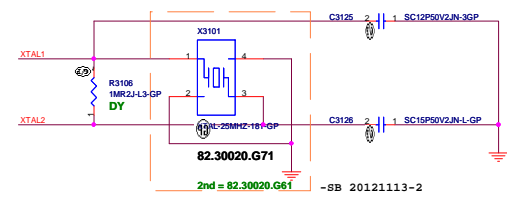
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Audio AMP		
Size	Document Number	Rev
A3	EA40 CX	-3
Date:	Thursday, June 06, 2013	Sheet 30 of 103



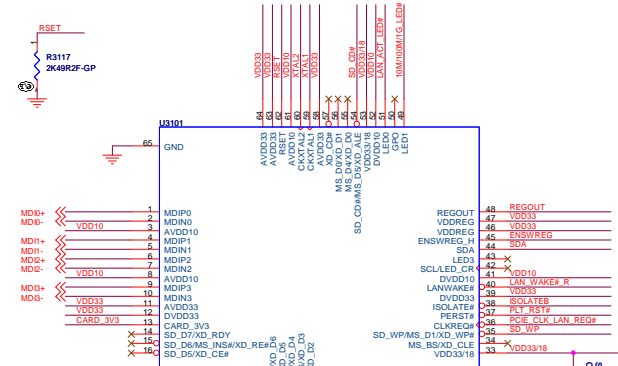
the Caps close to VDD33 pin

Close to VDDREG pin

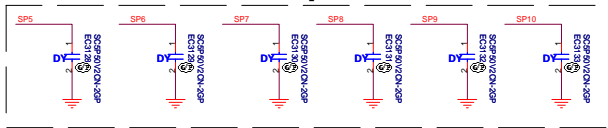
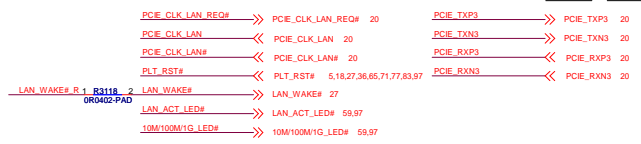
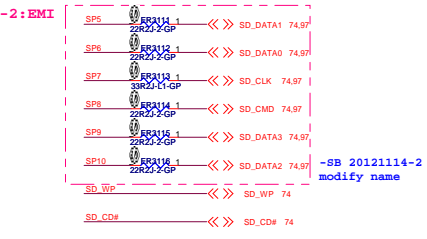
close to pin33 and pin53



SP1	SD D7	xD_RDY
SP2	SD D6	MS_INS#
SP3	SD D5	xD_CE#
SP4	SD D4	xD_WE#
SP5	SD D3	MS_CLK
SP6	SD D2	xD_D6
SP7	SD D1	MS_D7
SP8	SD D0	xD_D5
SP9	SD D0	MS_D3
SP10	SD D0	xD_D4
SP11	SD D0	MS_D6
SP12	SD D0	xD_D3
SP13	SD D0	MS_D2
SP14	SD D0	xD_D2
SP15	SD D0	MS_D1
SP16	SD D0	xD_D1



close the Pin 18-pin 23



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Title: **LAN(RTL8411)**

Size: Document Number: **EA40 CX** Rev: **-3**

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Title		
RTS5159 (CARD READER)		
Size	Document Number	Rev
Custom	EA40 CX	-3
Date: Thursday, June 06, 2013	Sheet 32	of 103

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Size

A4

Document Number

EA40 CX

Rev

-3

Date: Thursday, June 06, 2013

Sheet 33 of

103

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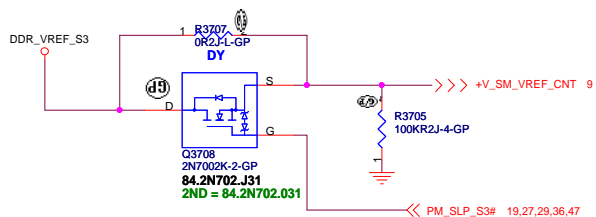
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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A4	EA40 CX		-3
Date: Thursday, June 06, 2013		Sheet 34 of	103

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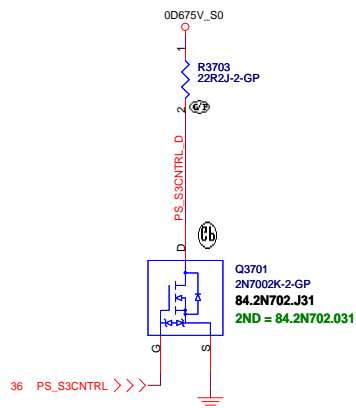
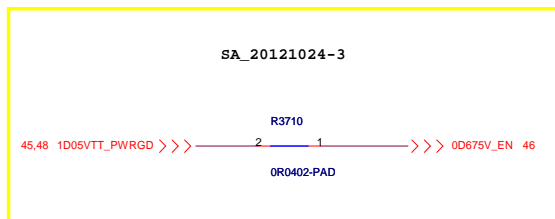
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緯創資通		Wistron Corporation	
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Title			
USB 3.0 Controller			
Size	Document Number	Rev	
Custom	EA40 CX	-3	
Date:	Thursday, June 06, 2013	Sheet	35 of 103

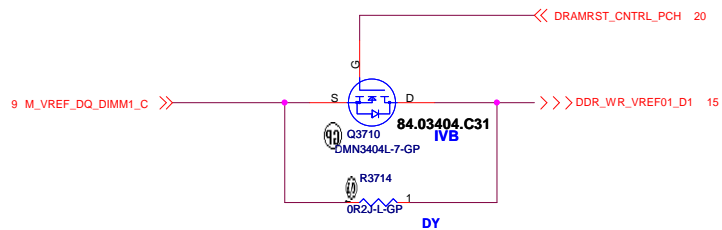
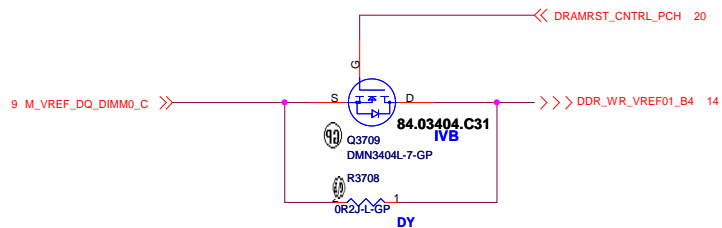
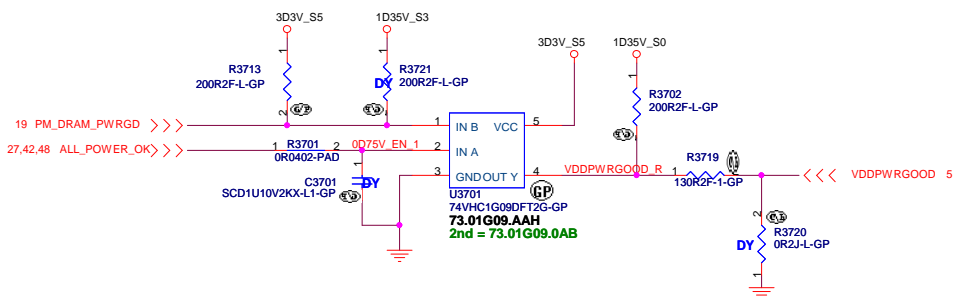
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



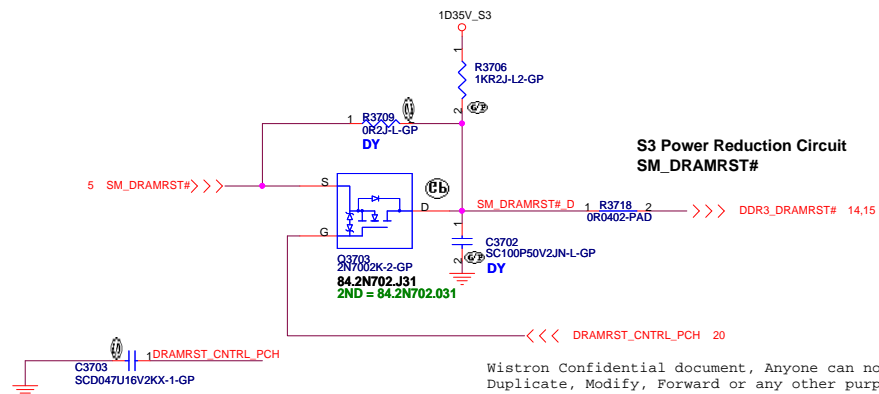
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

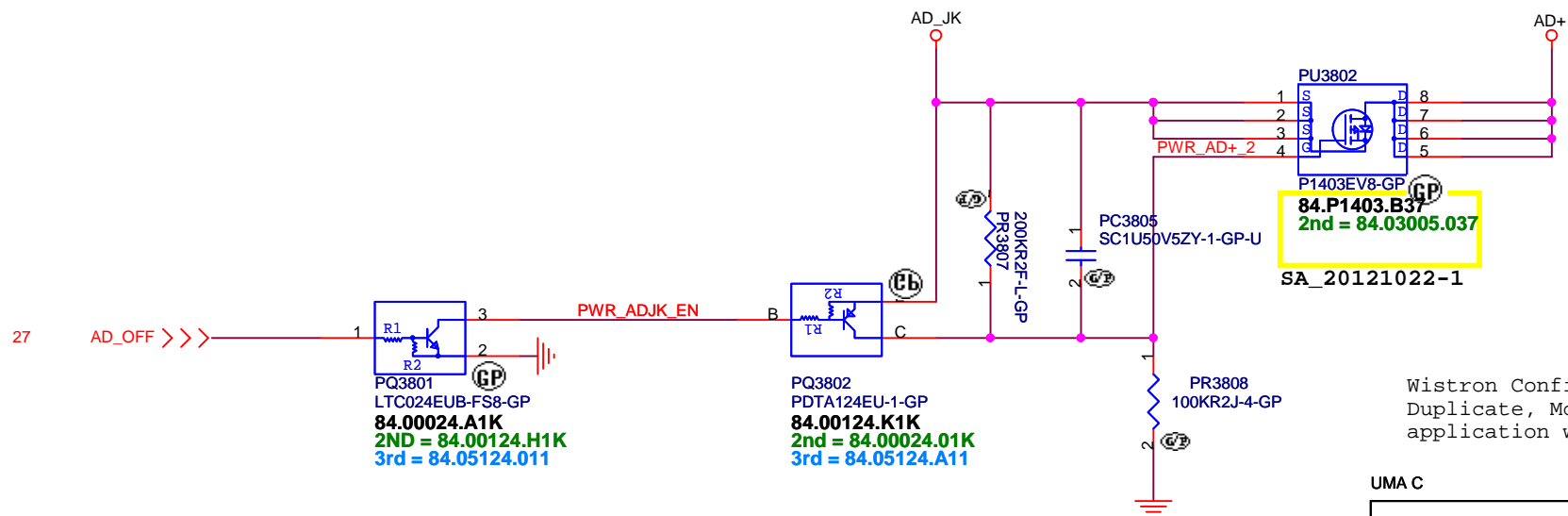
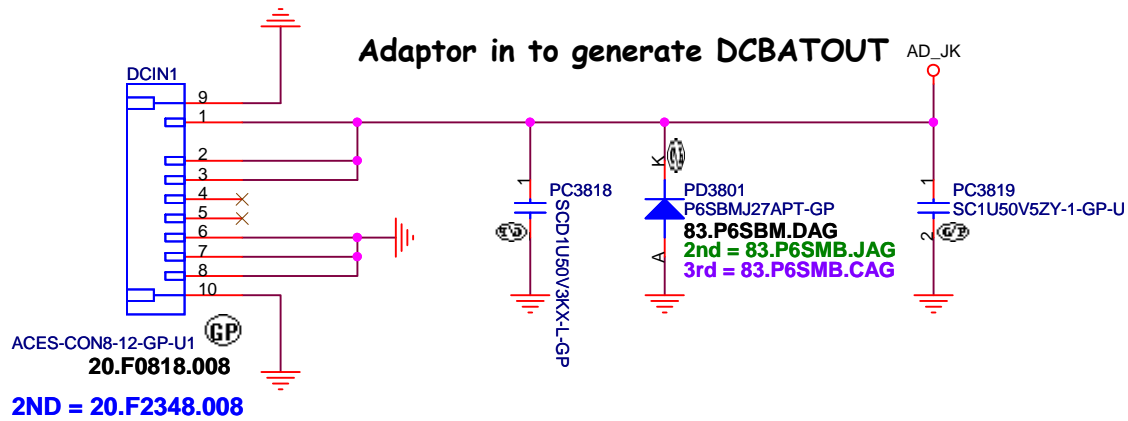


S3 Power Reduction Circuit
SM_DRAMRST#

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Title			
ADAPTER			
Size	Document Number	Rev	
Custom	EA40 CX	-3	
Date:	Thursday, June 20, 2013	Sheet	37 of 103



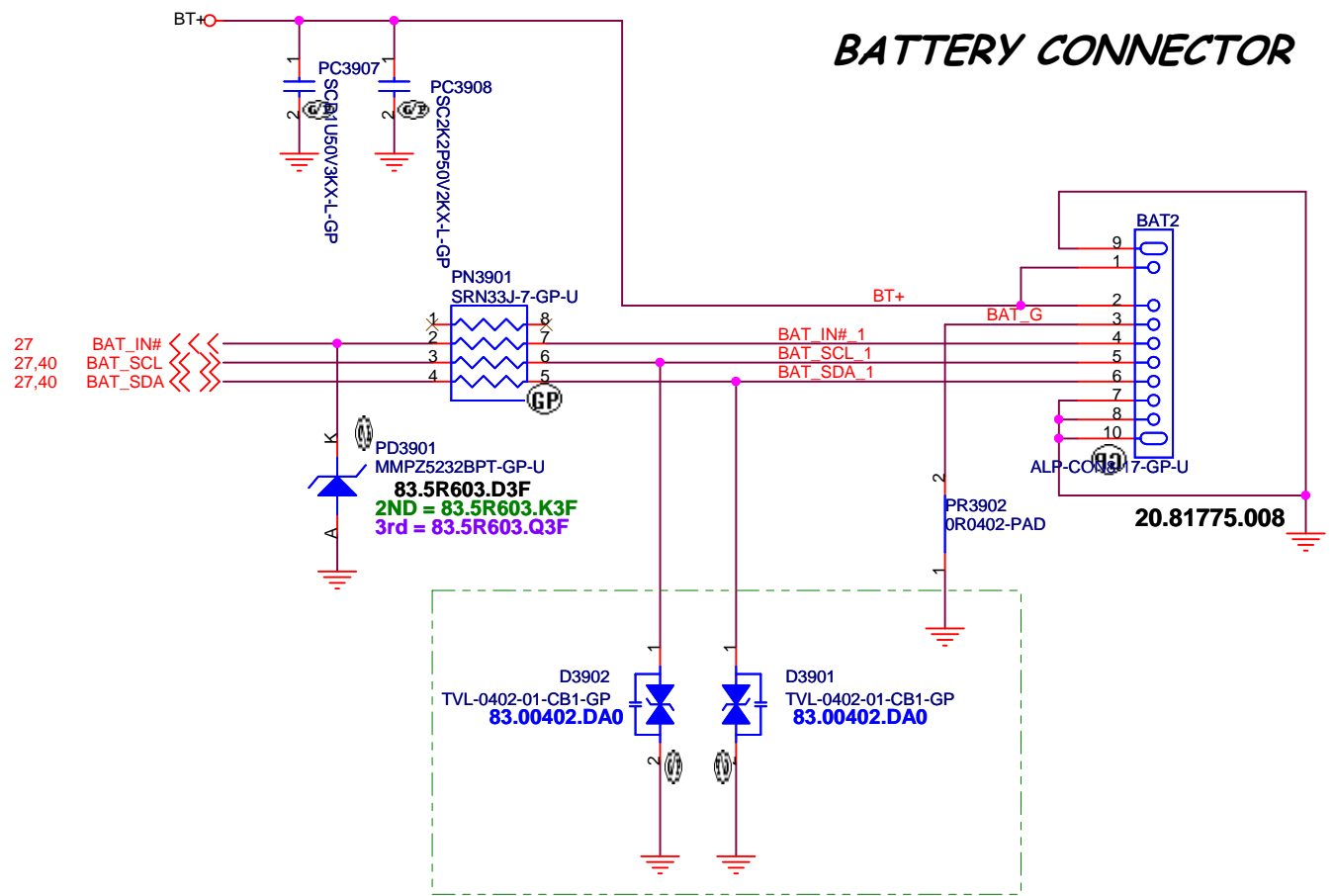
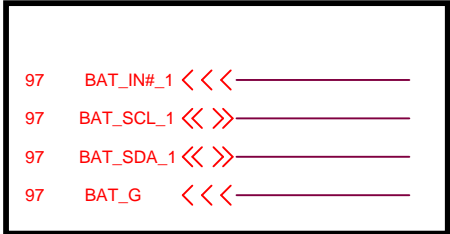
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Size	Document Number	Rev
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BATTERY CONNECTOR



BATTERY CONNECTOR

SC_20130205_AFR

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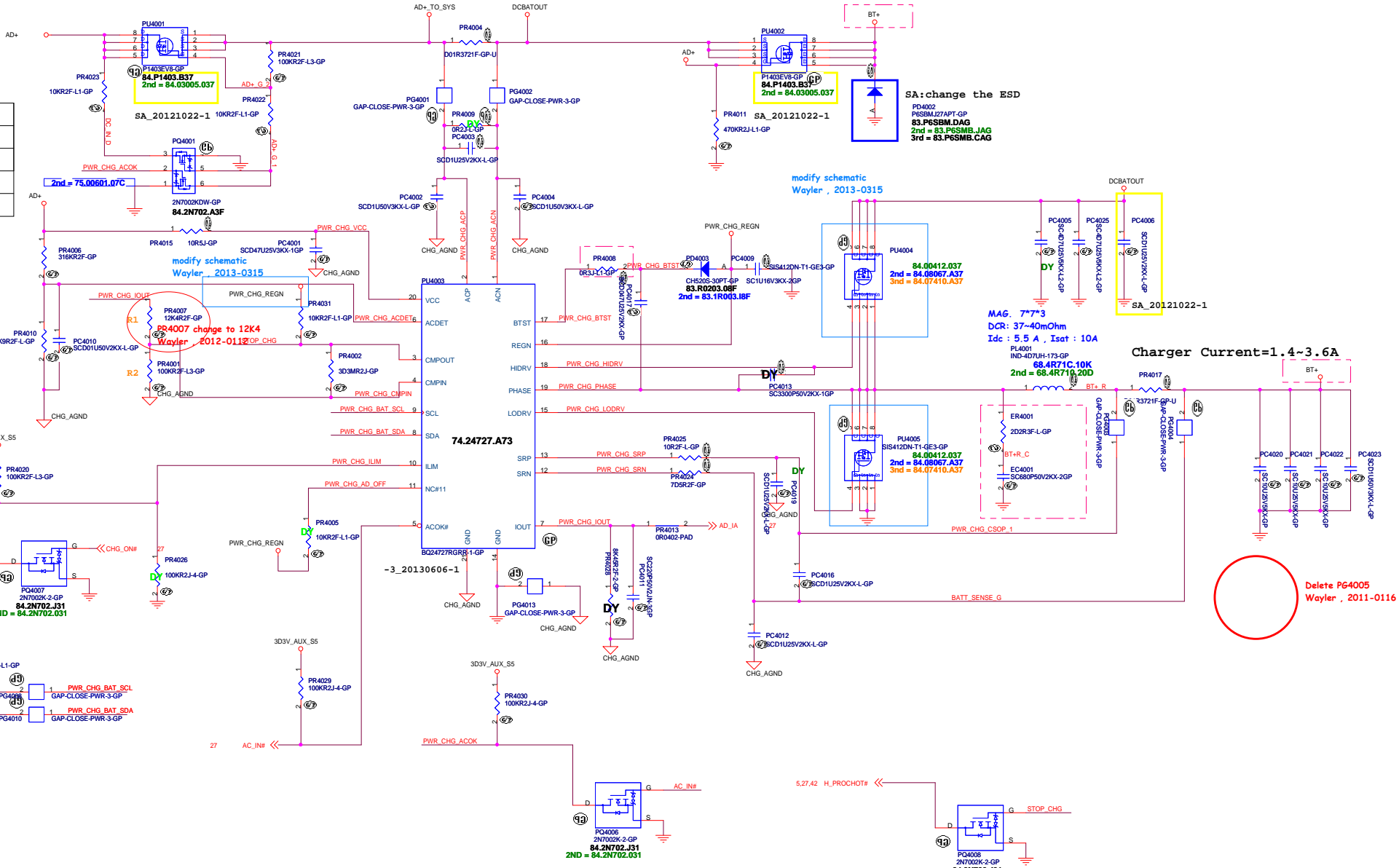
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Title BATT CONN			
Size A4	Document Number EA40 CX		Rev -3
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SSID = Charger

A8 (ANNIE/ASTRO)
PR4014, PR4016

AD+ total power	R1	R2
65w	1.2.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	1.18k	100K



MAG. 777*3
DCR: 37~40mOhm
I_{dc}: 5.5 A , I_{sat}: 10A
2nd = 68.4R71C.10K
3rd = 68.4R71C.20D

Charger Current=1.4~3.6A

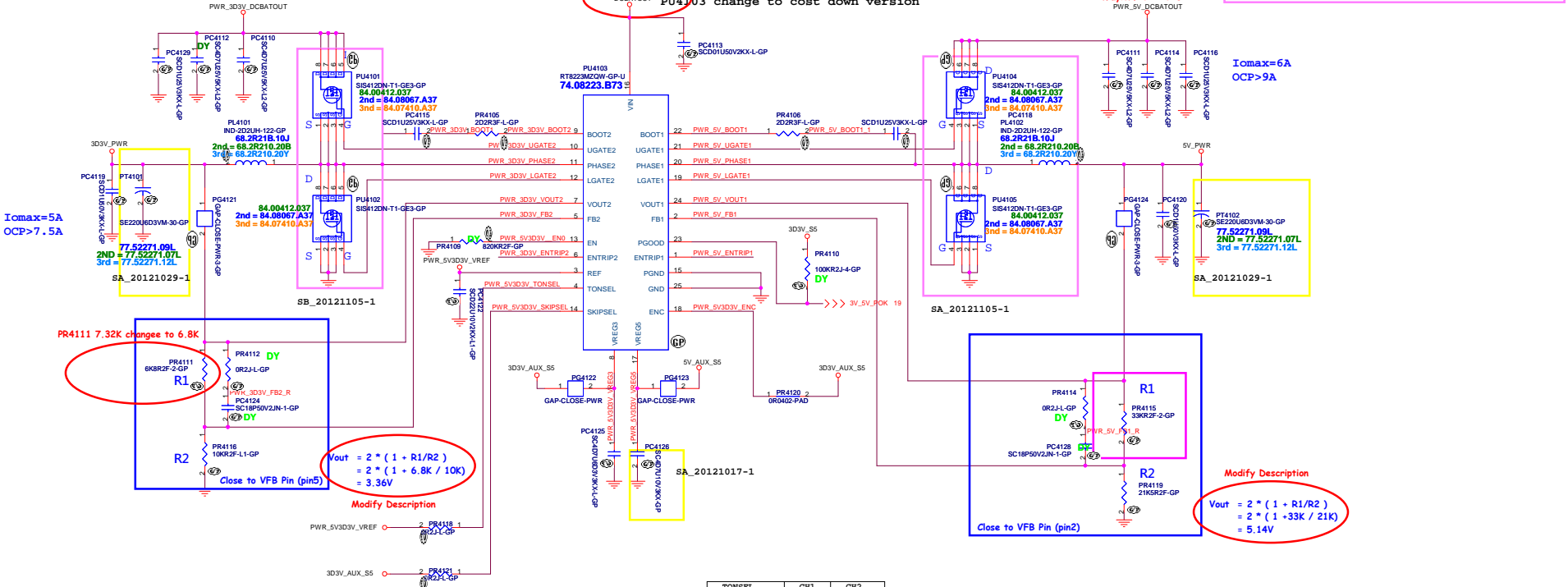
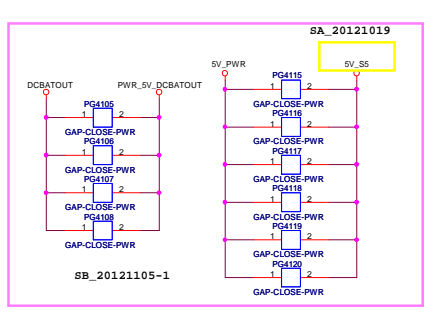
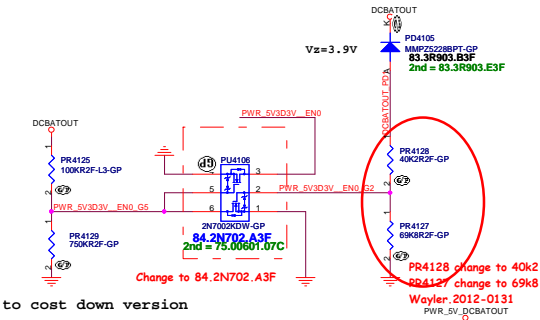
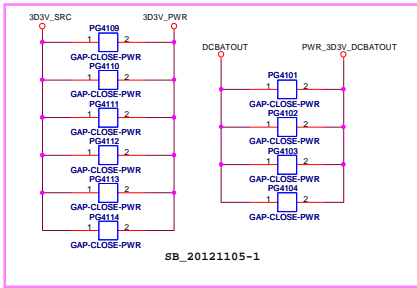
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Waylor, 2011-0116

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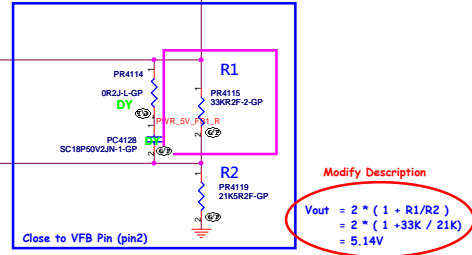
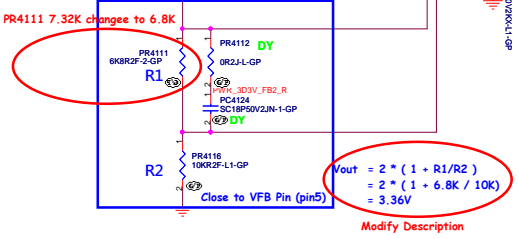
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Size	Document Number	Rev
Custom	EA40 CX	-3
Date	Friday, June 21, 2013	Sheet 40 of 103



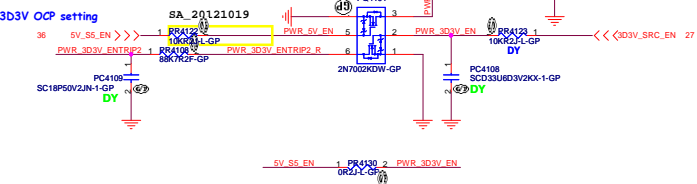
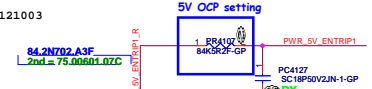
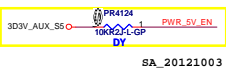
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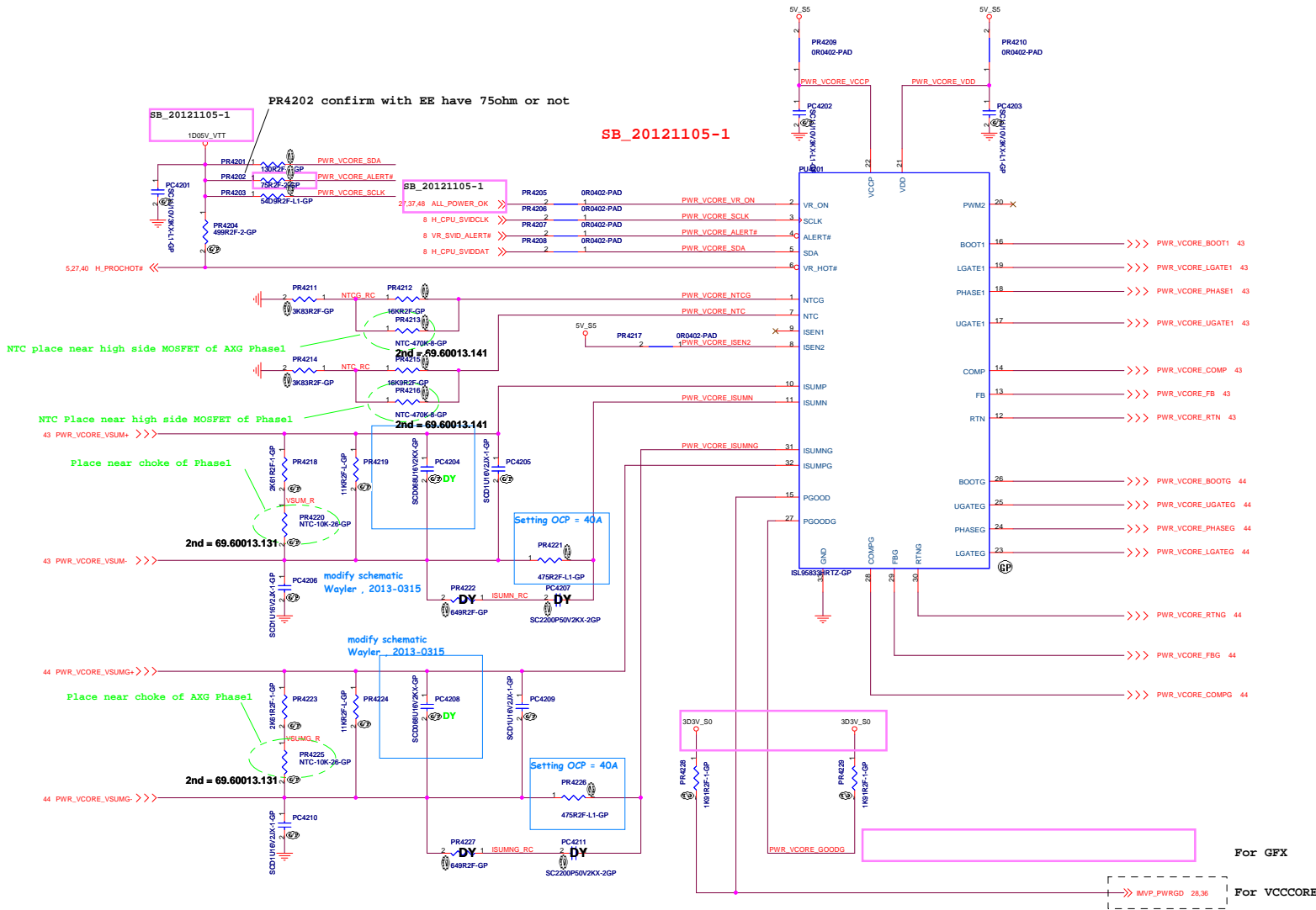


TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VRBG3 or VRBG5	400kHz	500kHz

SKIPSEL	VRBG3 or VRBG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only



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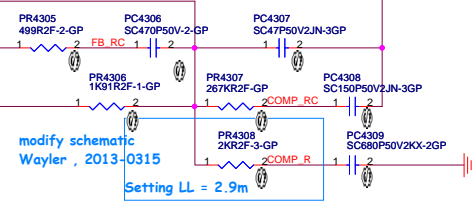
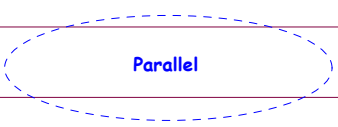
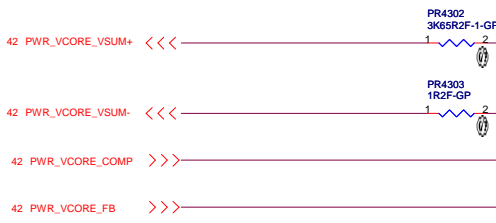
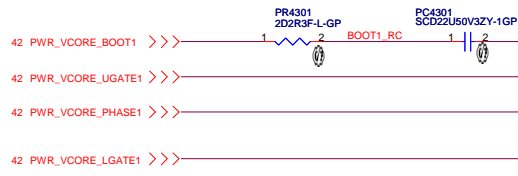
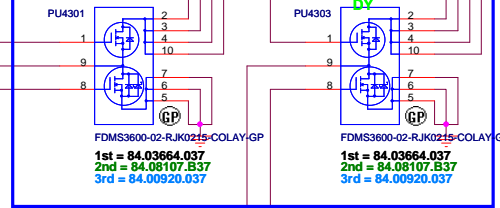


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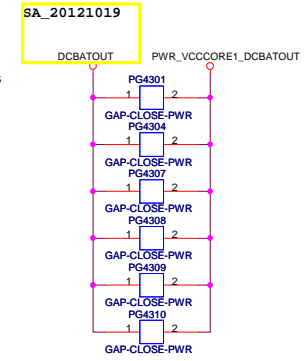
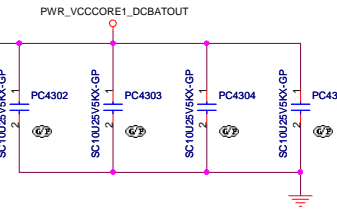
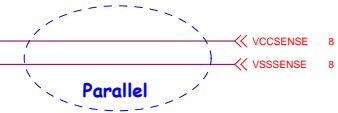
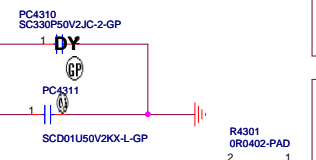
BOM control

	Main source	2nd source
PU4301	84.03664.037 (FDMS3664S)	Mount
PU4302	84.03664.037 (FDMS3664S)	DY

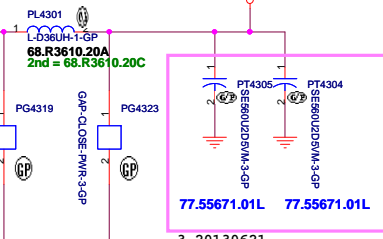
BOM control



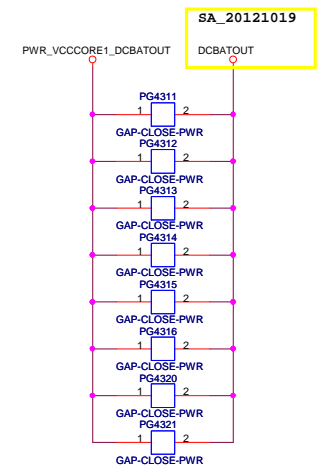
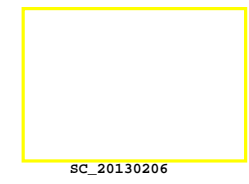
modify schematic
Wayler, 2013-0315
Setting LL = 2.9m



Pana . 10 x 10 x 4
DCR 1.1 mOhm
Isat : 24A



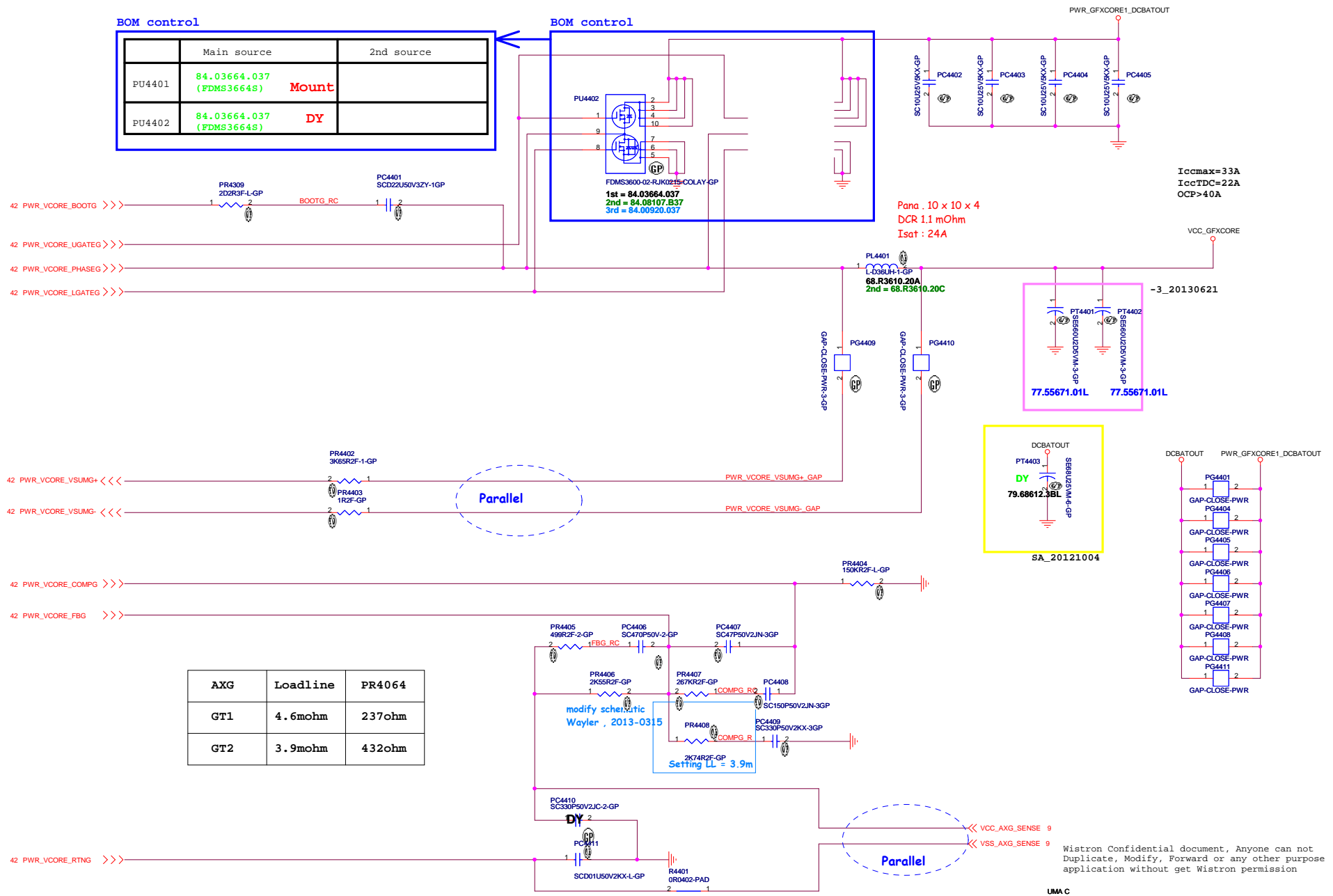
-3_20130621



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ISL95833_CPU_CORE(2/3)	
Size Custom	Document Number EA40 CX
Date: Friday, June 21, 2013	Sheet 43 of 103
Rev -3	



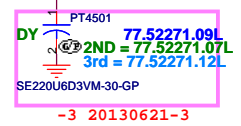
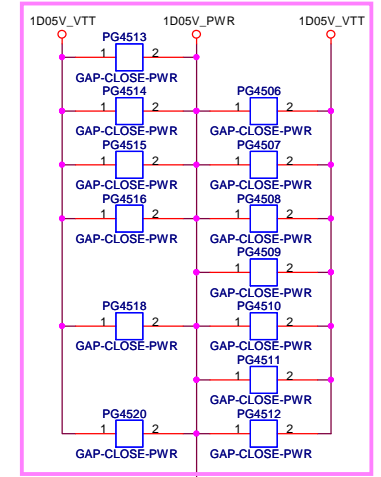
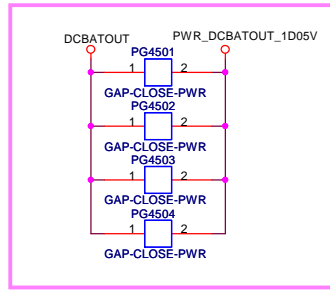
AXG	Loadline	PR4064
GT1	4.6mohm	237ohm
GT2	3.9mohm	432ohm

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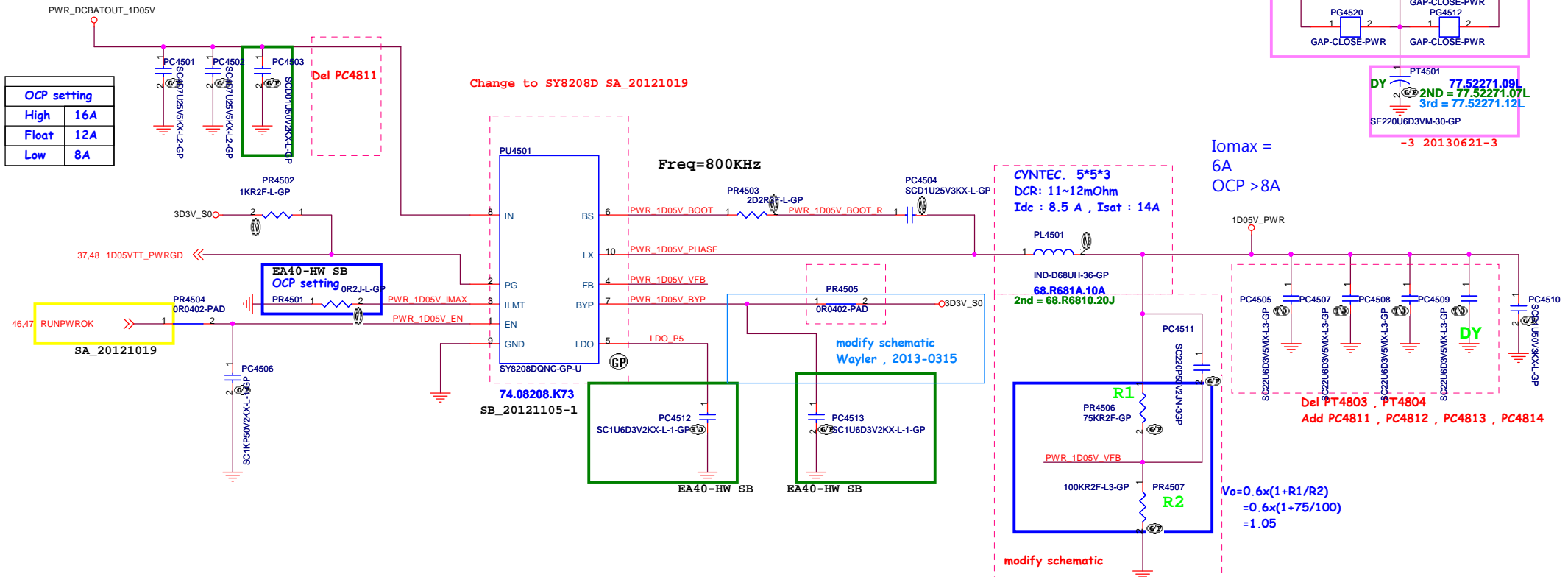
SY8208D for 1D05V

SB_20121105-1

SB_20121105-1



OCP setting	
High	16A
Float	12A
Low	8A



46.47 RUNPWOK SA_20121019

EA40-HW SB OCP setting

74.08208.K73 SB_20121105-1

Freq=800KHz

CYNTEC. 5*5*3
DCR: 11~12mOhm
Idc : 8.5 A , Isat : 14A

Iomax = 6A
OCP > 8A

$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 75/100) = 1.05$$

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UMA C

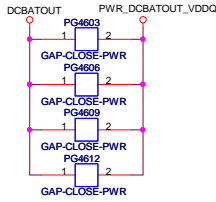
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1D05V(SY8208D)**

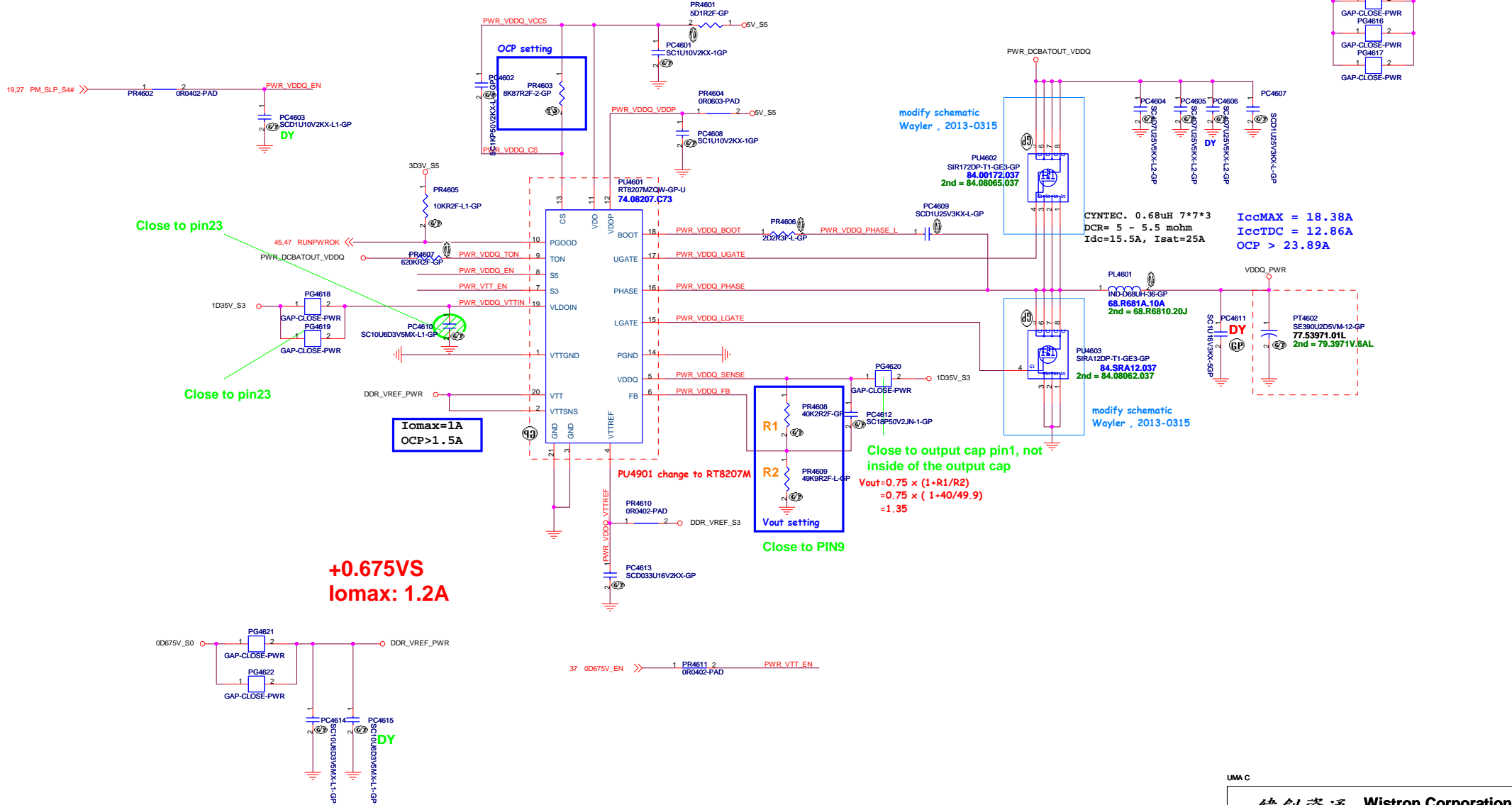
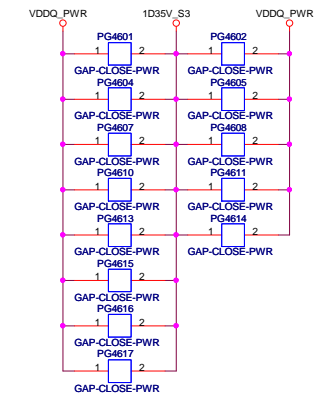
Size A3 Document Number: **EA40 CX** Rev: **-3**

Date: Friday, June 21, 2013 Sheet 45 of 103

SSID = PWR.Plane.Regulator_lp2v0p6v



RT8207L for VDDQ



Close to pin23

Iomax=1A
OCP>1.5A

+0.675VS
Iomax: 1.2A

R1
R2
Vout setting

Close to output cap pin1, not inside of the output cap
 $V_{out} = 0.75 \times (1 + R1/R2)$
 $= 0.75 \times (1 + 40/49.9)$
 $= 1.35$

modify schematic
Wayler, 2013-0315

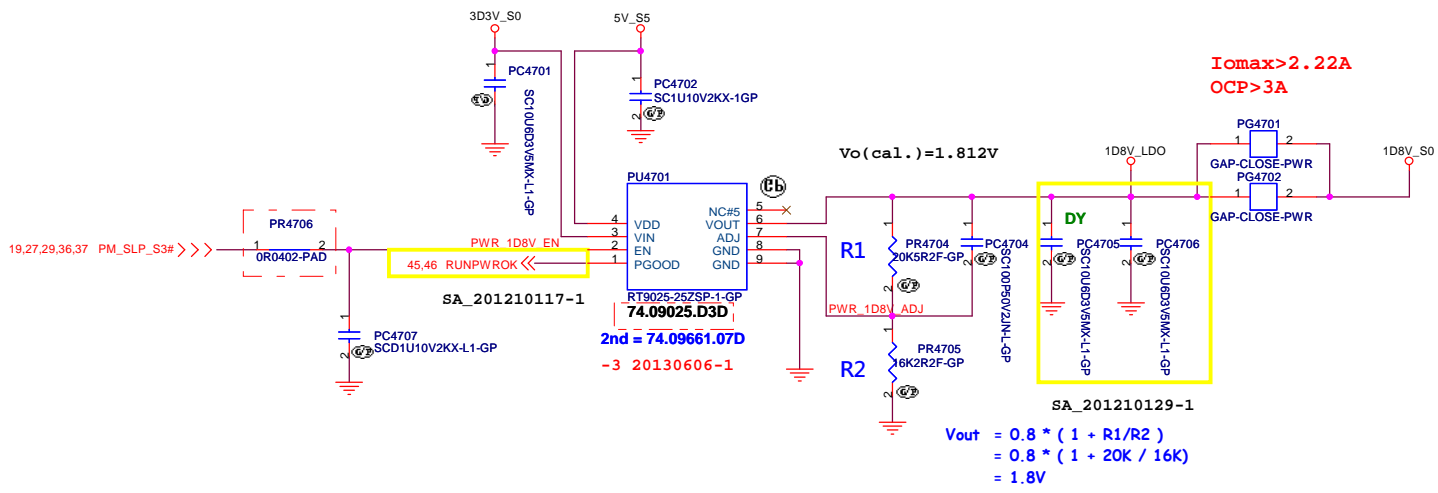
modify schematic
Wayler, 2013-0315

CYNTec. 0.68uH 7*7*3
DCR = 5 ~ 5.5 mohm
Idc=15.5A, Isat=25A

IccMAX = 18.38A
IccTDC = 12.86A
OCP > 23.89A

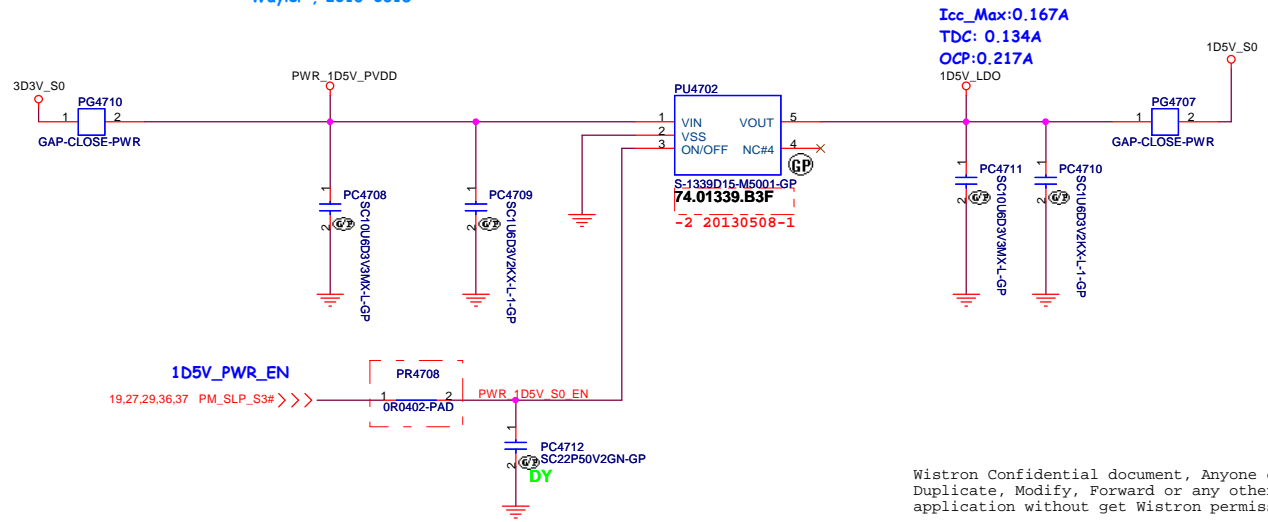
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



S-1339D15 for 1D5V_S0

modify schematic
Wayler , 2013-0315

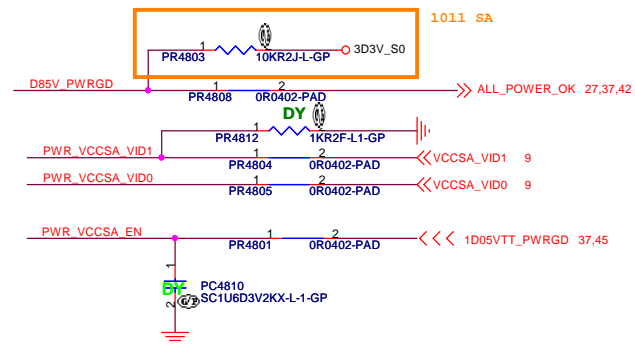


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Title			
LDO 1D8V&1D5V(RT9025)			
Size	Document Number	Rev	
Custom	EA40 CX	-3	
Date:	Thursday, June 20, 2013	Sheet	47 of 103

LDO G978 for VCCSA



D0, D1 V₀ Selection Table

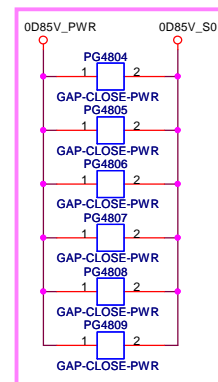
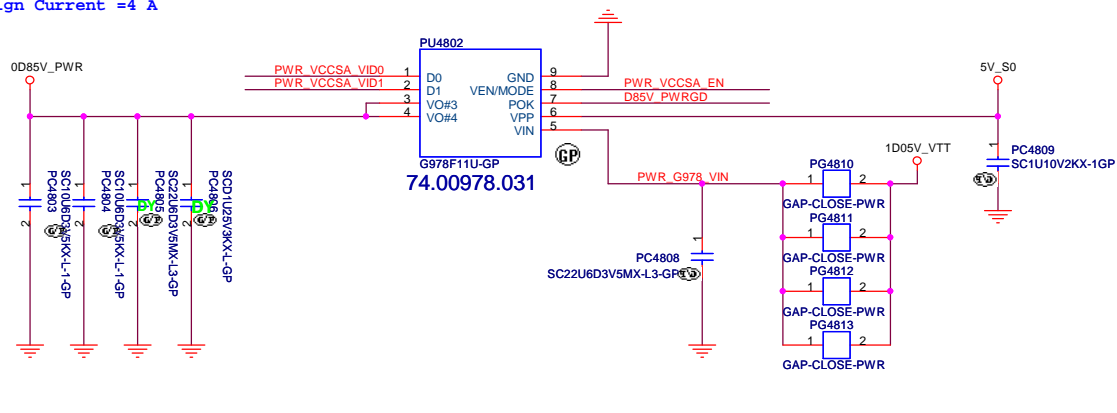
D0	D1	V ₀ MODE=0	V ₀ MODE=1
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

"x" means "don't care".

VEN/MODE Logic

VEN/MODE (VPP=5V)	EN logic	VEN/MODE (VPP=5V)	MODE logic
<0.6V	0	<2.0V	0
>1.0V	1	>2.6V	1

Design Current = 4 A

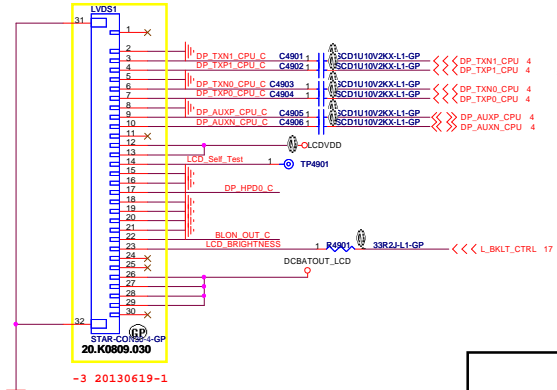


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Title: VCCSA LDO G978	
Size: A3	Document Number: EA40_CX
Date: Thursday, June 20, 2013	Rev: -3
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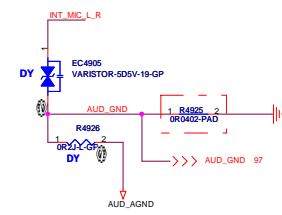
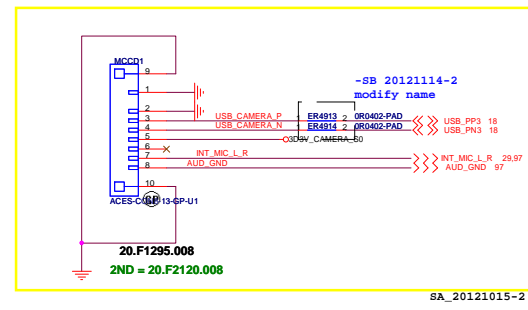
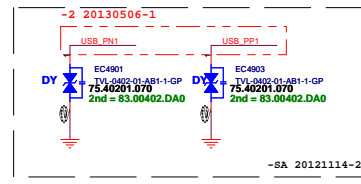
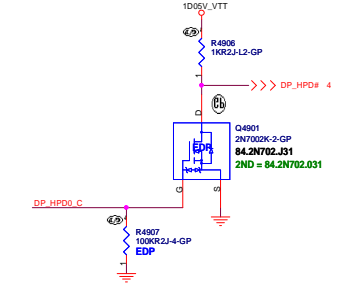
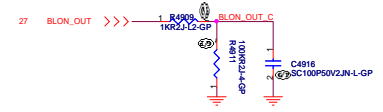
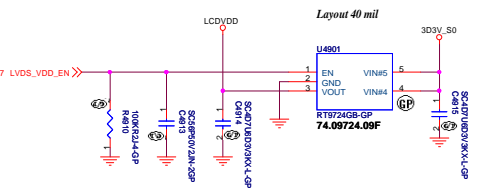
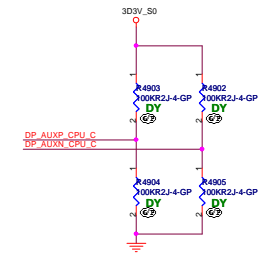
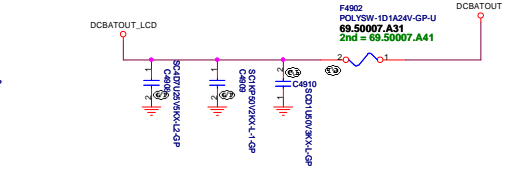
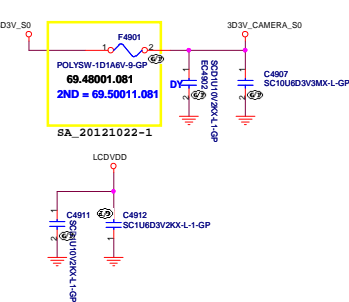
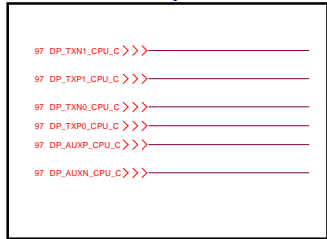
eDP Conn.



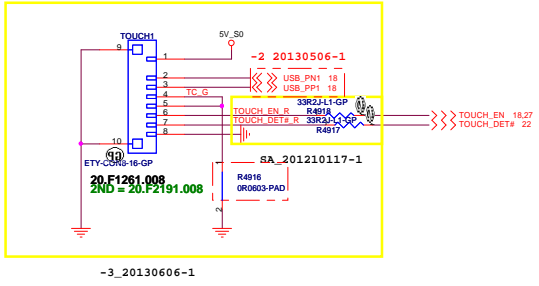
BY cable
 L(pin5 GND):DMIC
 H(pin5:floating):AMIC

For TestPoint

97 DP_HPDD_C >>>
 97 BLON_OUT_C >>>
 97 LCD_BRIGHTNESS >>>

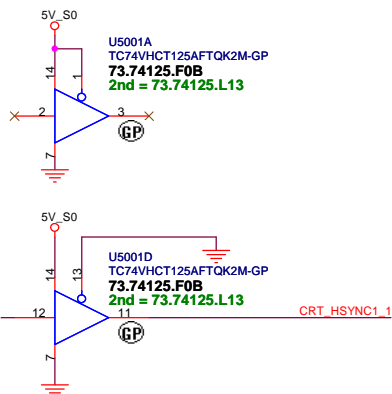
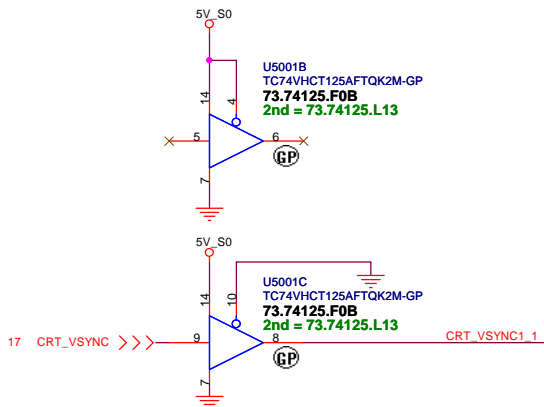
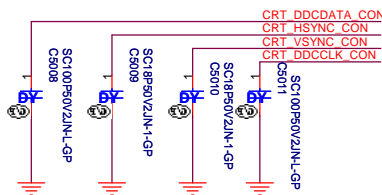
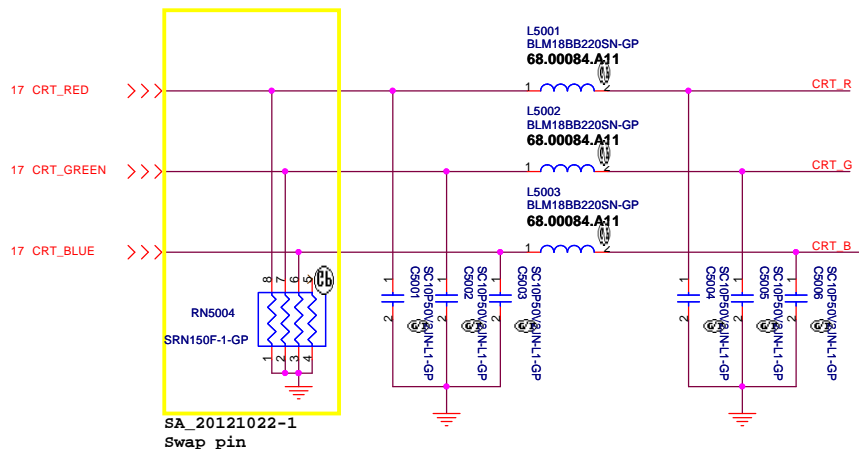
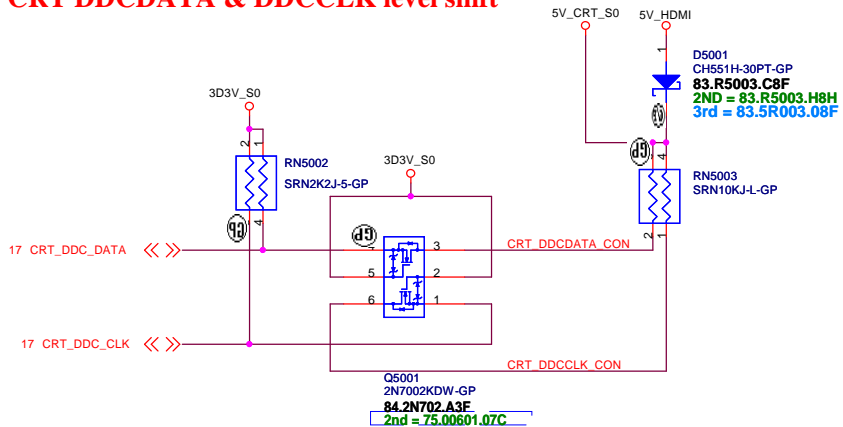
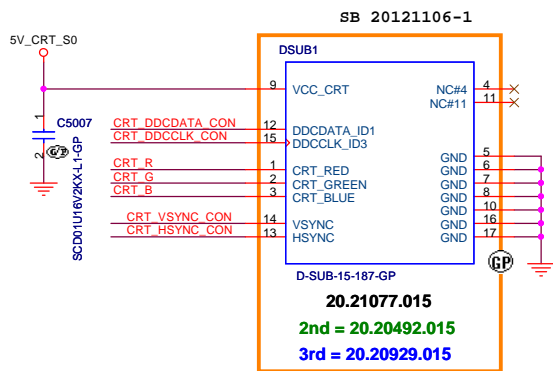


Touch Conn.



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CRT DDCDATA & DDCCLK level shift



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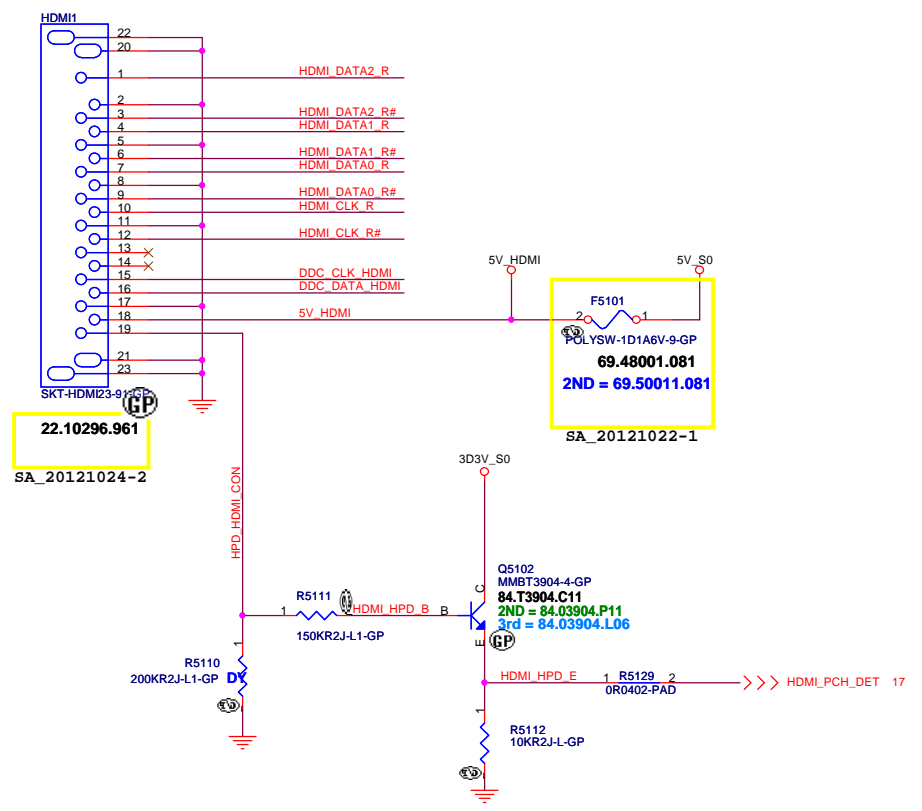
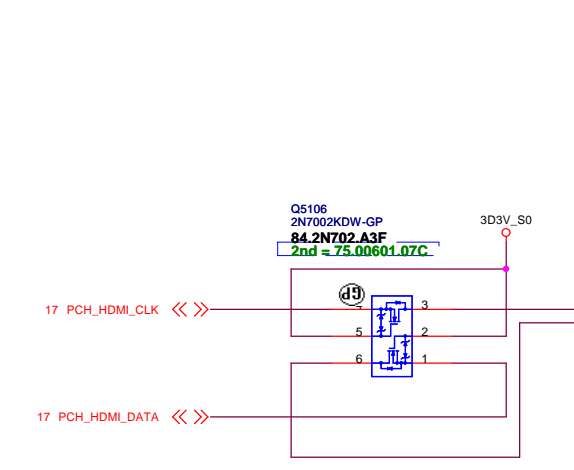
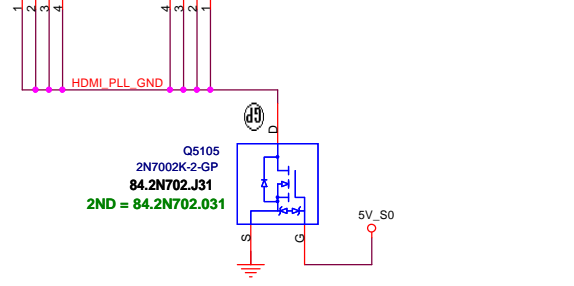
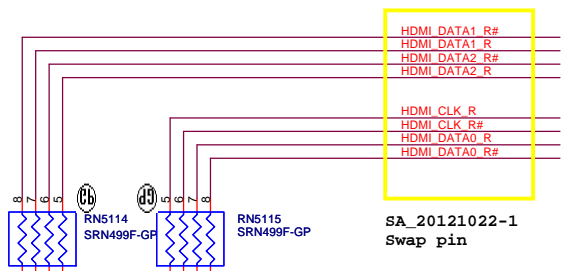
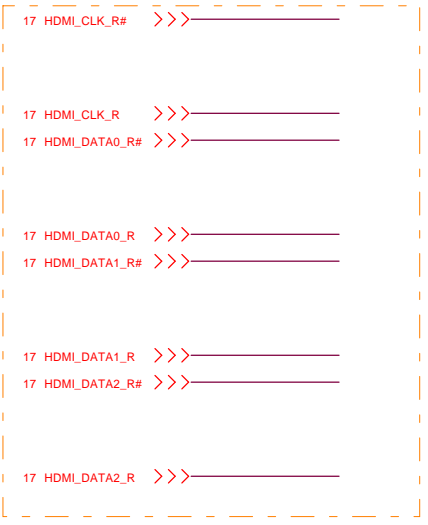
UMA C		
緯創資通 Wistron Corporation		
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Title		
CRT Connector		
Size A3	Document Number	Rev
	EA40 CX	-3
Date: Thursday, June 20, 2013	Sheet 50 of 103	

SSID = VIDEO HDMI Level Shifter & CONNECTOR

Close to HDMI Connector

change = DIS:499 ohm
Fist = UMA Muxless:680 ohm

-1_20130315A



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LED BACKLIGHT CONVERTER POWER

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Title		
eDP		
Size	Document Number	Rev
A3	EA40 CX	-3
Date:	Thursday, June 06, 2013	Sheet 52 of 103

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Title			
S-VIDEO			
Size	Document Number		Rev
A4	EA40 CX		-3
Date:	Thursday, June 06, 2013	Sheet 53	of 103

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Title

Reserved

Size
A4

Document Number

EA40 CX

Rev
-3

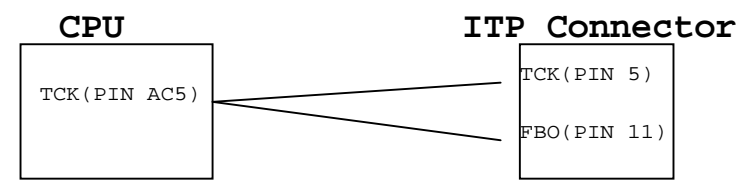
Date: Thursday, June 06, 2013

Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

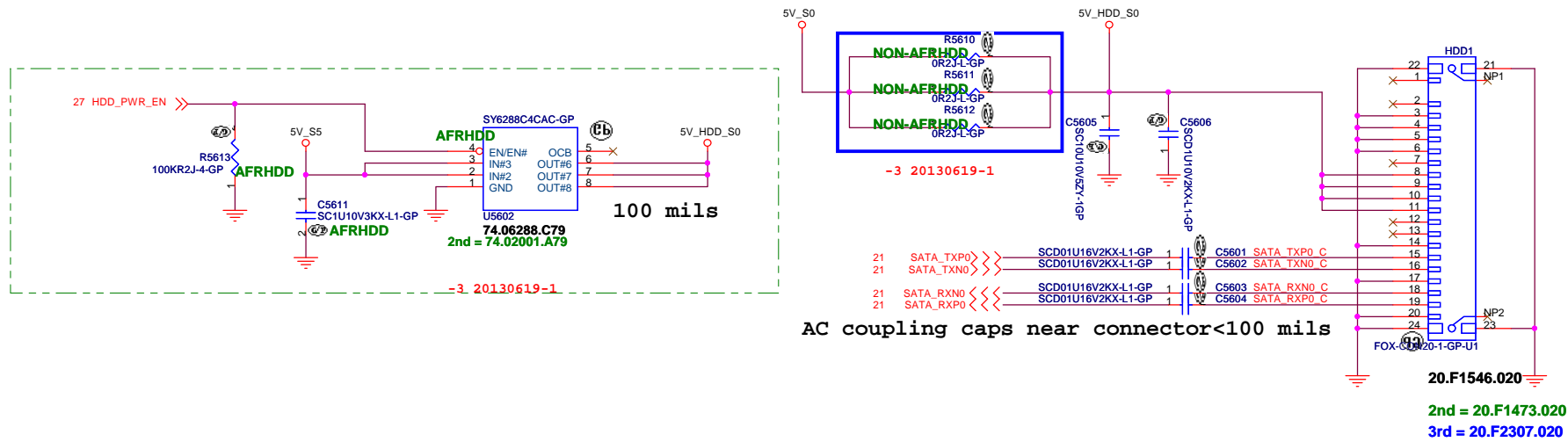


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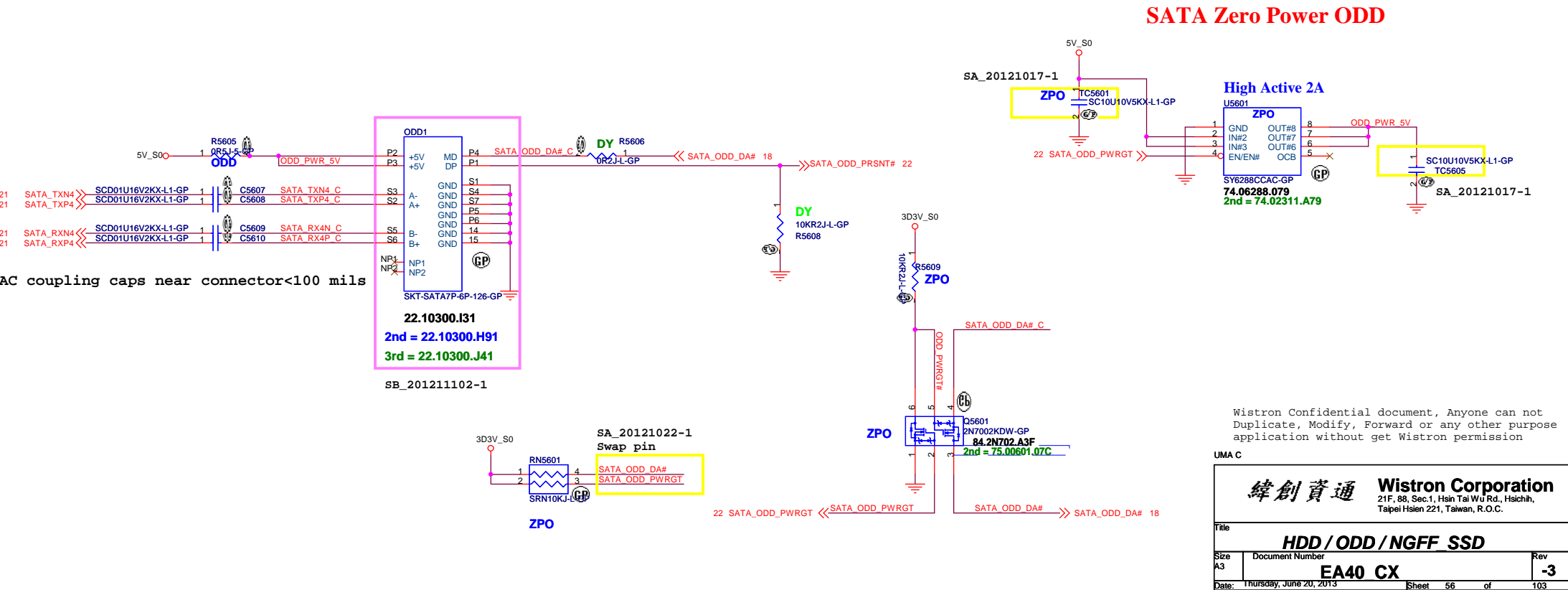
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Title			
ITP			
Size	Document Number		Rev
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Date: Thursday, June 06, 2013		Sheet 55	of 103

SATA HDD Connector



ODD Connector



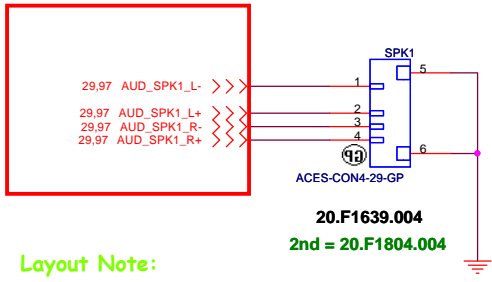
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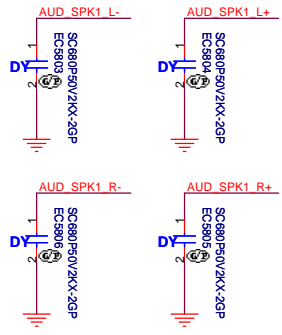
Title		
E-SATA/USB CHARGER		
Size	Document Number	Rev
A3	EA40 CX	-3
Date:	Thursday, June 06, 2013	Sheet 57 of 103

SSID = AUDIO *Speaker*

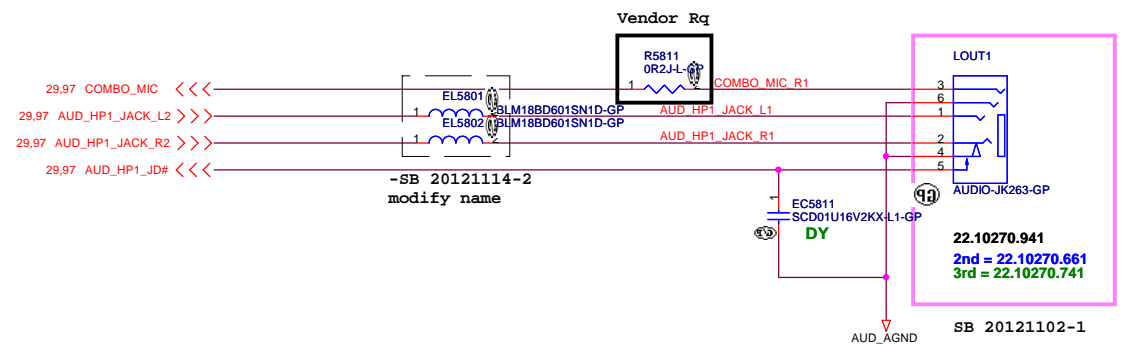


Layout Note:

Trace width=40mil



Combo Jack

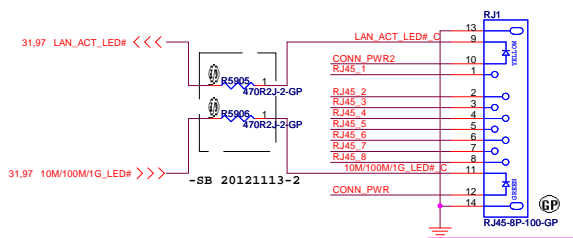
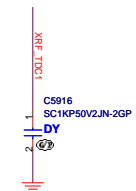
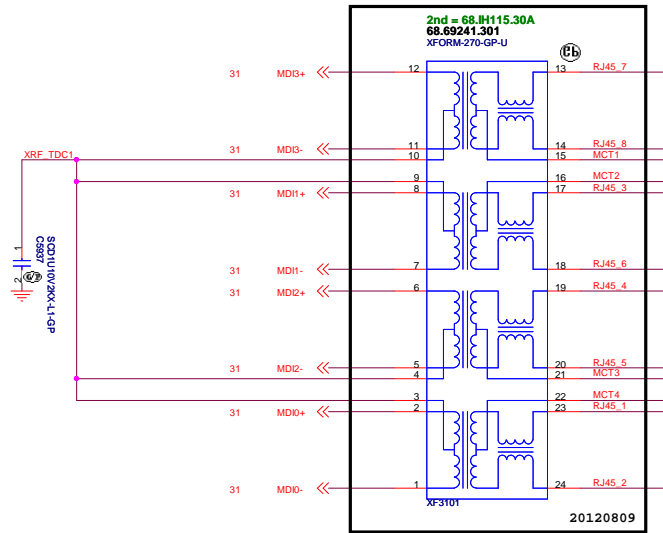


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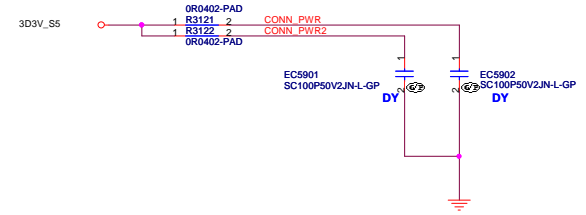
UMA C

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Title		
Audio Jack		
Size A3	Document Number	Rev
	EA40 CX	-3
Date: Thursday, June 06, 2013	Sheet 58 of 103	

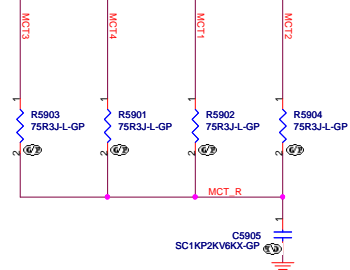
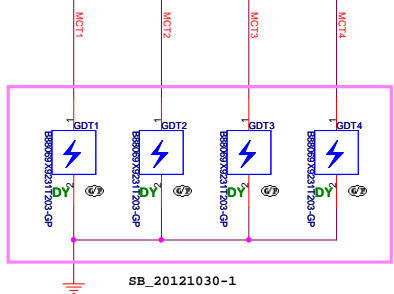
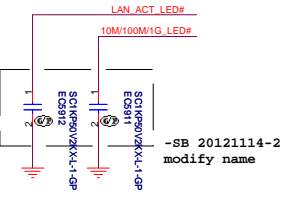
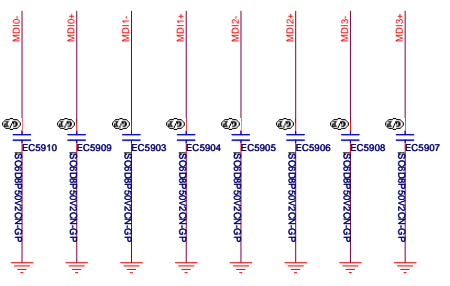
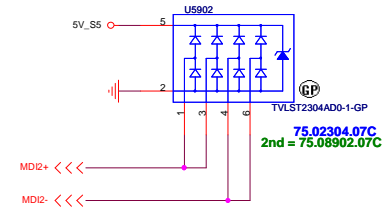
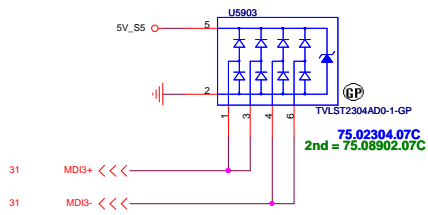
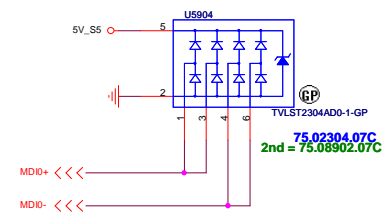
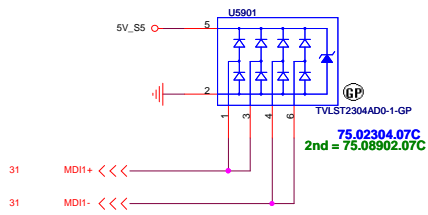
SSID = LAN



2nd 22.10327.141 wait to verify
-3_20130606-1



- 97 RJ45_1 >>>
- 97 RJ45_2 >>>
- 97 RJ45_3 >>>
- 97 RJ45_4 >>>
- 97 RJ45_5 >>>
- 97 RJ45_6 >>>
- 97 RJ45_7 >>>
- 97 RJ45_8 >>>
- 31.97 LAN_ACT_LED# >>>
- 31.97 10M/100M1G_LED# >>>
- 97 CONN_PWR >>>
- 97 CONN_PWR2 >>>



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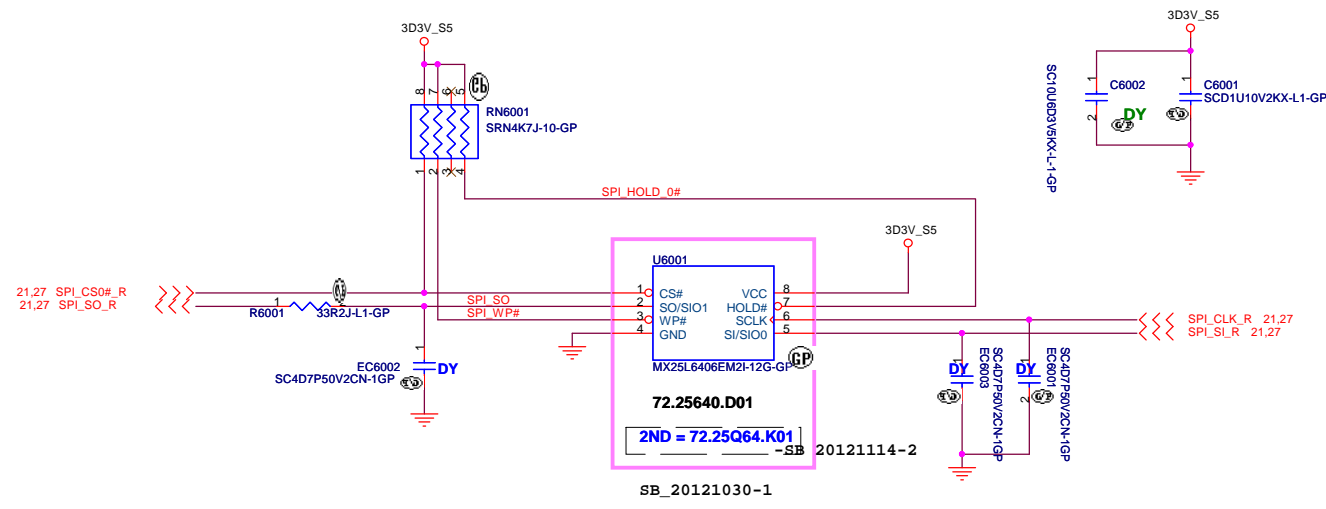
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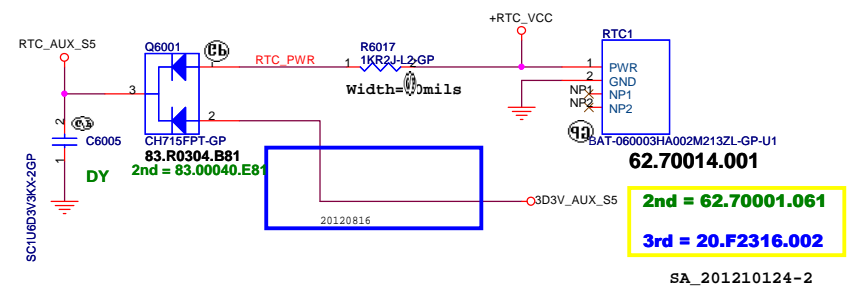
Title: LAN CONNECTOR
Size: Custom
Date: Thursday, June 20, 2013

Document Number: EA40 CX
Rev: -3
Sheet 59 of 103

SSID = Flash.ROM



SSID = RTC



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Title Flash/RTC		
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SSID = USB

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USB Power SW		
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SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

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Title		
Bluetooth		
Size A4	Document Number EA40 CX	Rev -3
Date: Thursday, June 06, 2013		Sheet 63 of 103

D

D

C

C

B

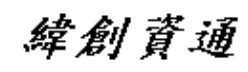
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A

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SSID = Wireless

Mini Card Connector(WWAN)

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Title **WWAN Connector**

Size A4	Document Number EA40 CX	Rev -3
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Title

Reserved

Size

A4

Document Number

EA40 CX

Rev

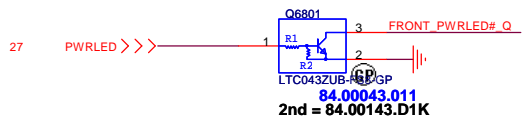
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Date: Thursday, June 06, 2013

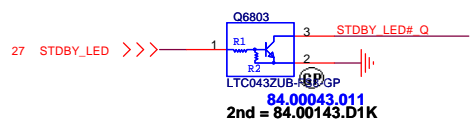
Sheet 67 of 103

SSID = User.Interface

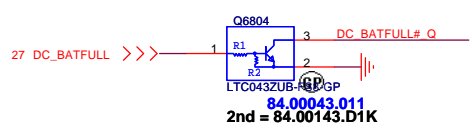
Power button LED



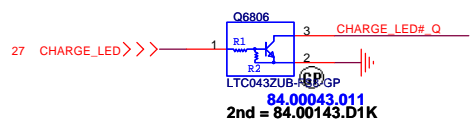
Power STDBY_LED



Battery LED2(DC_BATFULL)

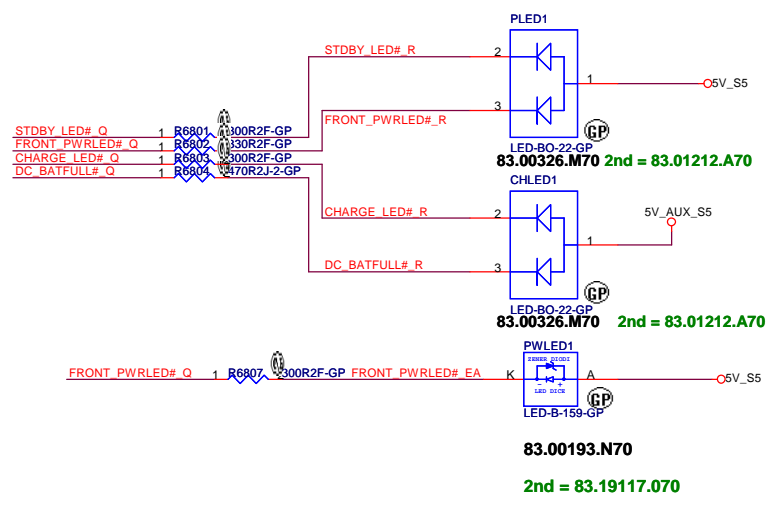
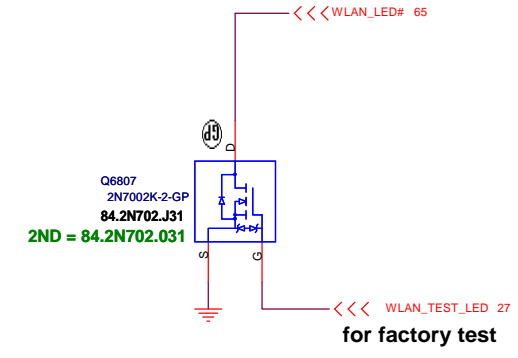


Battery LED1(CHARGE)

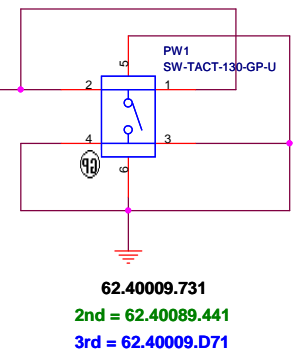
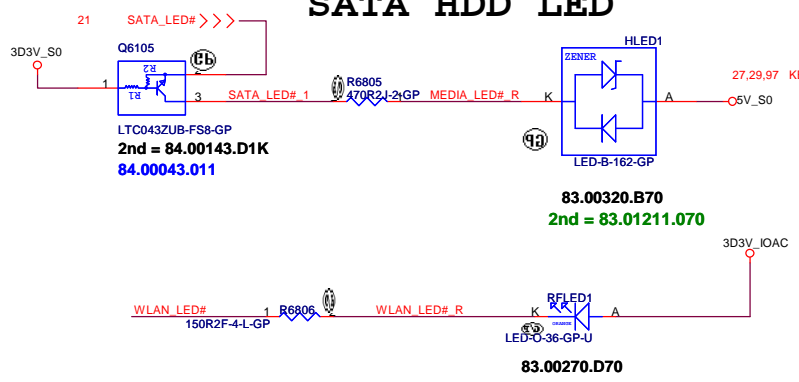


WLAN_LED

From module



SATA HDD LED

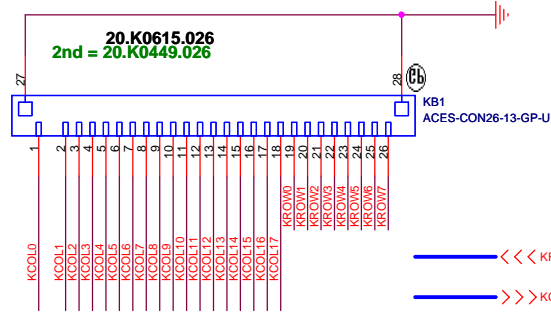


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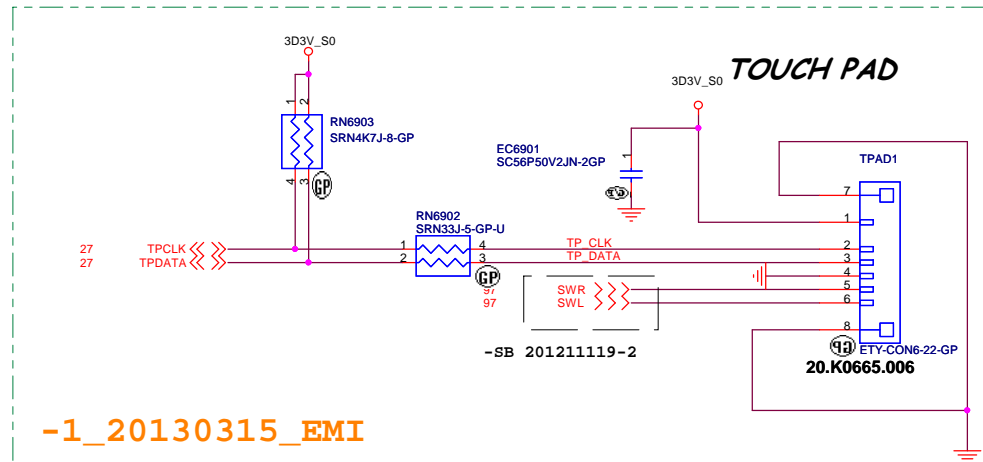
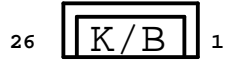
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Title			
LED Bard/Power Button			
Size	Document Number	Rev	
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SSID = KBC

Internal KeyBoard Connector

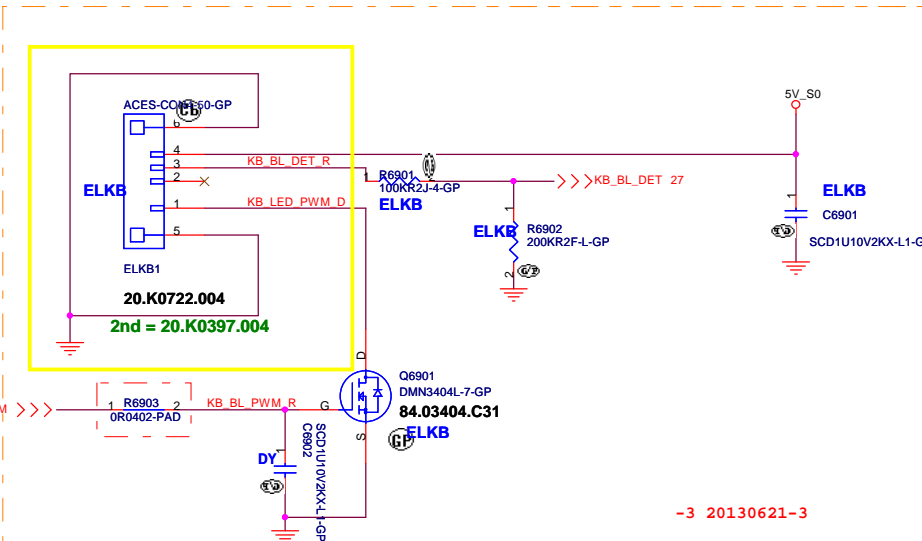
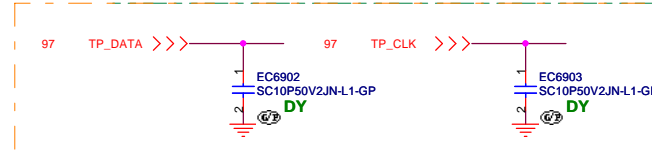


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

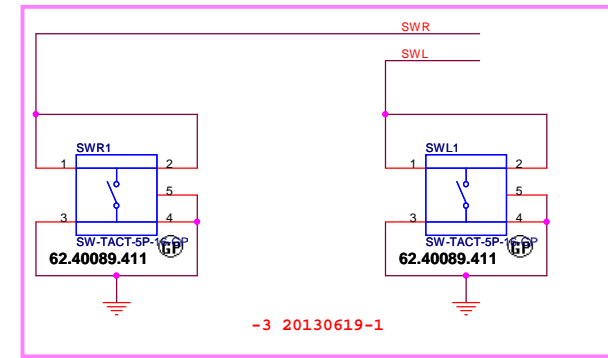


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SC_20130204_SWAP

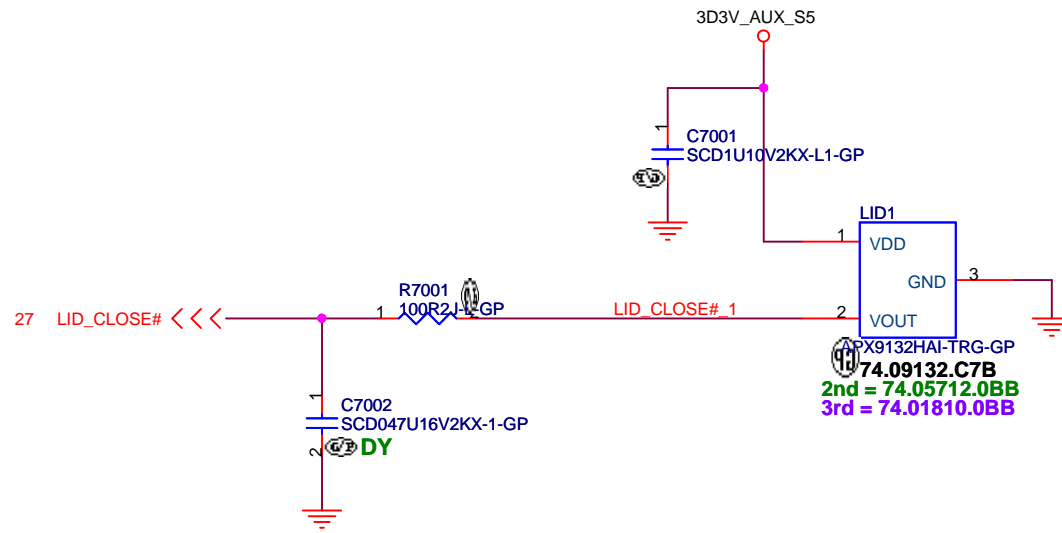


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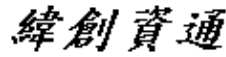
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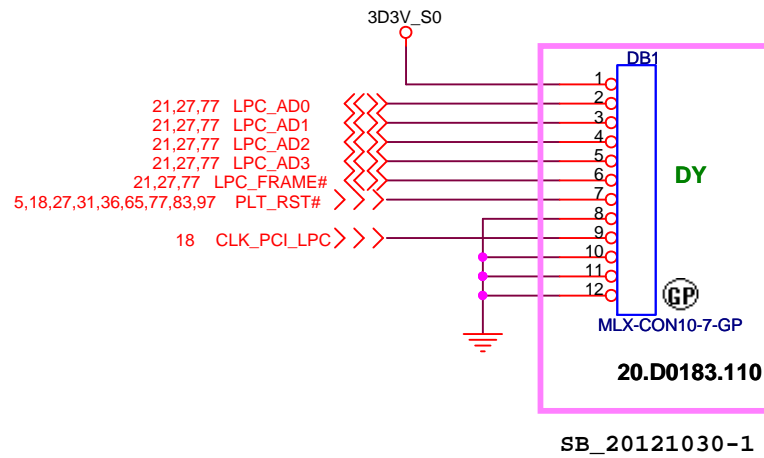
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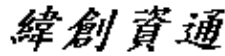
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Hall Sensor		
Size A4	Document Number EA40 CX	Rev -3
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Title <i>Dubug connector</i>		
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Size
A3

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Document Number

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A3

EA40 CX

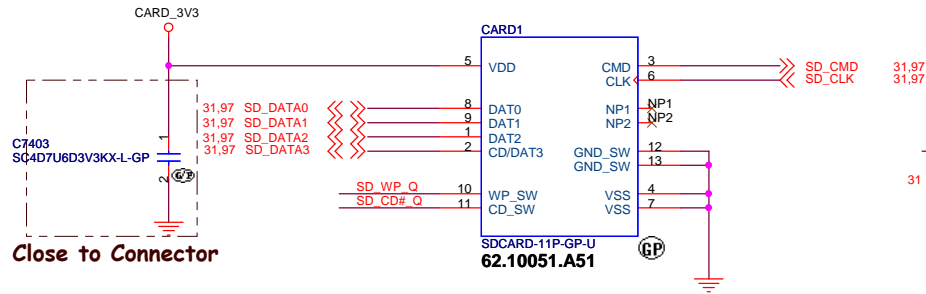
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Date: Thursday, June 06, 2013

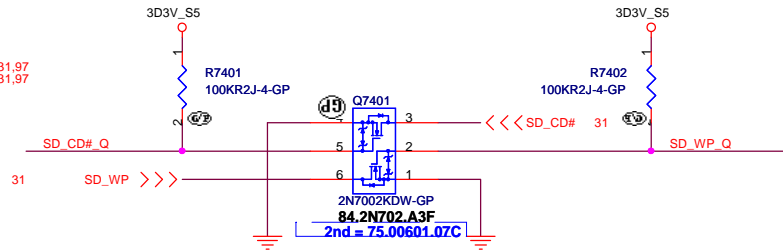
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SSID = SDIO

SD/MMC Card Reader



Close to Connector

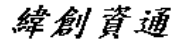


97 SD_WP_Q >>> _____
 97 SD_CD#_Q >>> _____

SP1	SP1	SD_D7	MS_INS#	xD_RDY
SP2	SP2	SD_D6	MS_INS#	xD_RE#
SP3	SP3	SD_D5	MS_INS#	xD_CE#
SP4	SP4	SD_D4	MS_INS#	xD_WE#
SP5	SP5	SD_D1	MS_CLK	xD_D6
SP6	SP6	SD_D0	MS_D7	xD_D5
SP7	SP7	SD_CLK	MS_D3	xD_D4
SP8	SP8	SD_CMD	MS_D6	xD_D3
SP9	SP9	SD_D3	MS_D2	xD_D2
SP10	SP10	SD_D2	MS_D2	xD_D7
SP11	SP11	MS_BS	MS_BS	xD_CLE
SP12	SP12	SD_WP	MS_D1	xD_WP#
SP13	SP13	SD_CD#	MS_D5	xD_ALE
SP14	SP14	MS_D4	MS_D4	xD_D0
SP15	SP15	MS_D0	MS_D0	xD_D1
SP16	SP16			xD_CD#

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Card Reader CONN		
Size Custom	Document Number EA40 CX	Rev -3
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SSID = ExpressCard

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Title		
New Card		
Size	Document Number	Rev
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Title

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Size

A4

Document Number

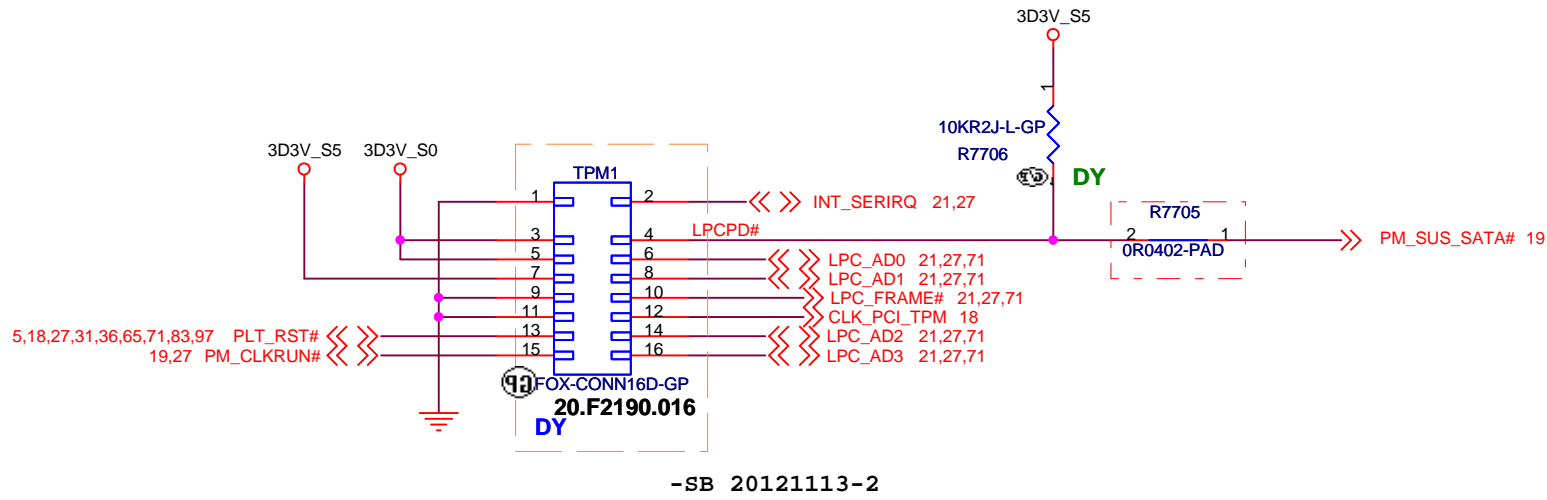
EA40 CX

Rev

-3

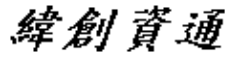
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TPM		
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SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Title			
G- Sensor			
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D

D

C

C

B

B

A

A

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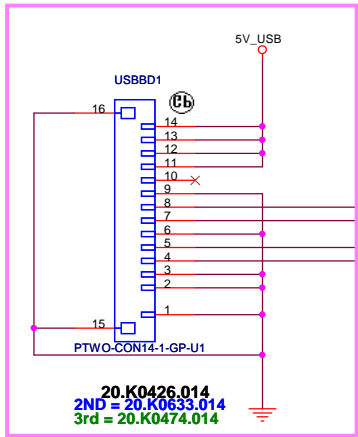
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Title	Reserved	
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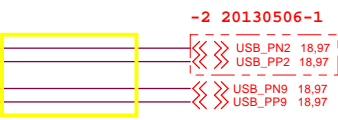
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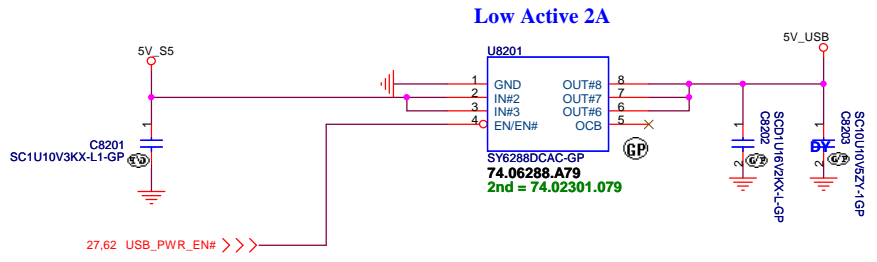


20.K0426.014
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 3rd = 20.K0474.014

SB 20121102-1



-2 20130506-1
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 USB_PP2 18,97
 USB_PN8 18,97
 USB_PP8 18,97

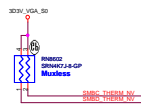
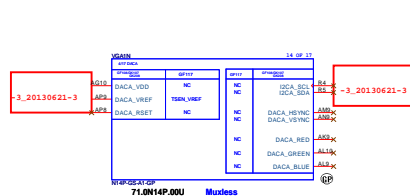


Low Active 2A

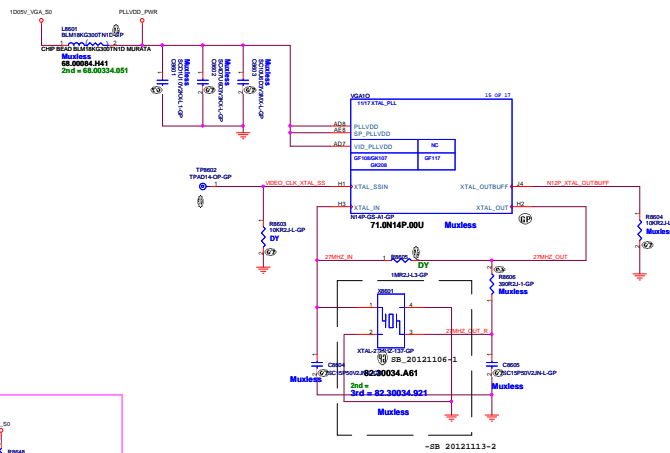
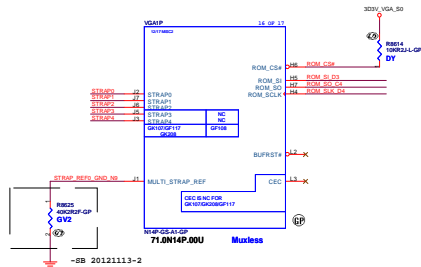
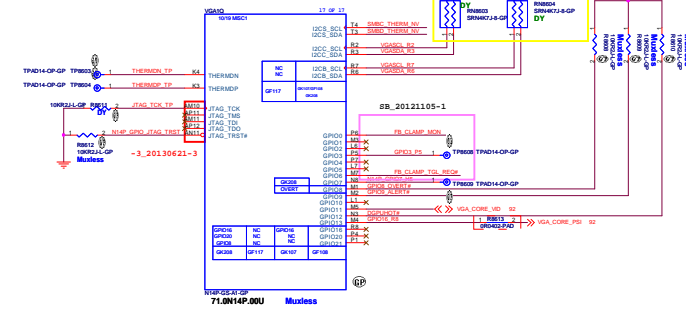
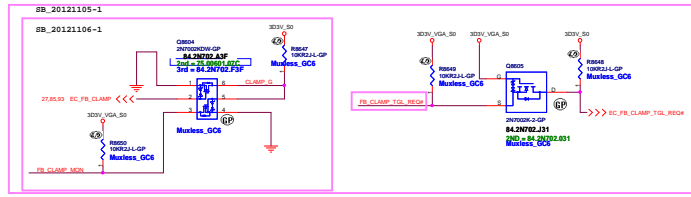
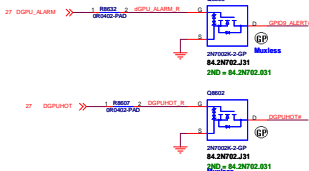
U8201
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Title		
IO Board Connector		
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unknown function



- 64.49915.6DL
- 64.10025.1.0L
- 64.15023.6DL
- 64.20025.6DL
- 64.24925.6DL
- 64.30125.6DL
- 64.34825.6DL
- 64.45325.6DL

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

- 4.99Kohm
- 10Kohm
- 15Kohm
- 20Kohm
- 24.9Kohm
- 30.1Kohm
- 34.8Kohm
- 45Kohm

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Data Code Minimum	Status
128Mx16 DDR3	Micron	0x0	1.5 V / 1.5 V	MT41J128M16JF-10Y3C-K	1000	1214	Production ready
	Samsung	0x5	1.5 V / 1.5 V	K4V2G1644E-BC1A	1000	1204	Production ready
	Hynix	0x6	1.5V / 1.5V	H5TQ2G63DFR-11C	900	11/A	Production ready
		0xC	1.5V / 1.5V	H5TQ2G63DFR-11C	900	11/A	Production ready
				H5TC2G63FFR-11C	1000	11/A	Production ready

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDQ	Manufacturer Part Number	Max Speed (MHz)	Memory Data Code Minimum	Status
256Mx16 DDR3	Samsung	0x0	1.5 V / 1.5 V	K4V4G1644E-HC11	900	N/A	Production ready
	Micron	0x0	1.5 V / 1.5 V	MT41H256M16HA-10Y3E	900	N/A	Production ready
	Hynix	0x3	1.5V / 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TQ4G63AFR-11C	N/A	N/A	Full production candidate

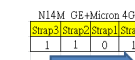
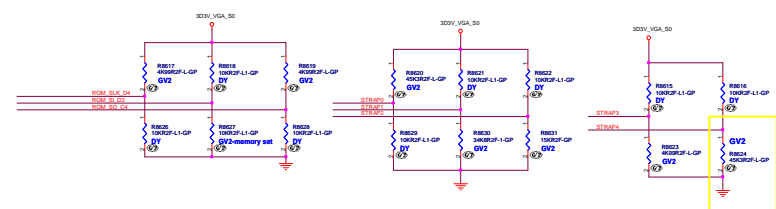
N14M-GE use Binary Strap. Please see the below information.

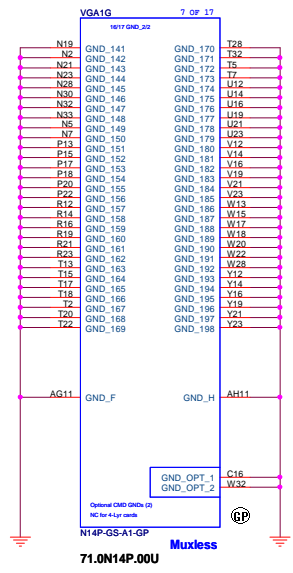
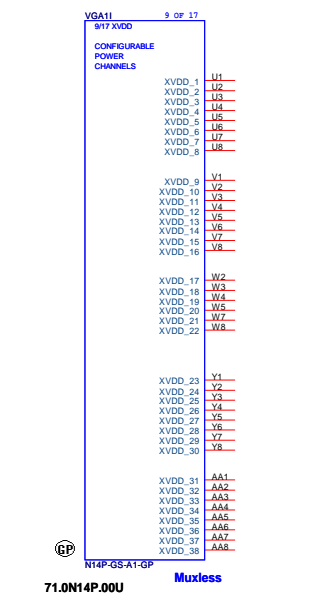
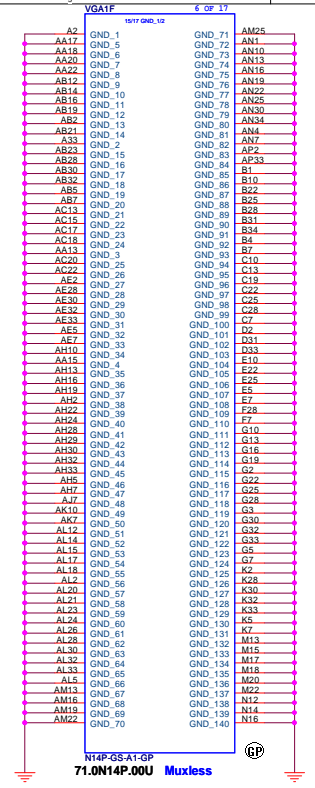
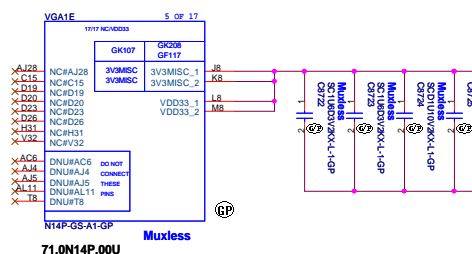
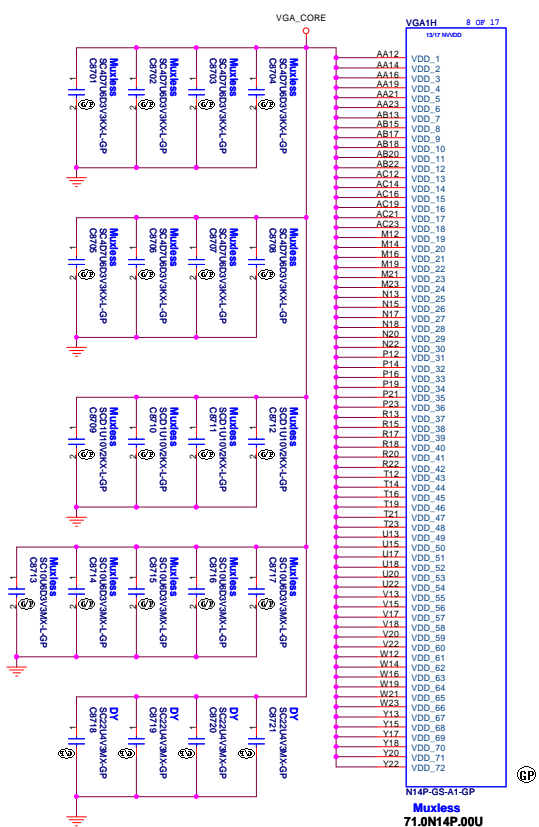
Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10K Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10K Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10K Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10K Ω	See Note below
STRAP1	RAM_CFG[1]	10K Ω	See Note below
STRAP2	RAM_CFG[2]	10K Ω	See Note below
STRAP3	RAM_CFG[3]	10K Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10K Ω	Pull-down to GND

N14P-GV2 Strap Pin Name	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP 1	3G10_PADCFG[3]	3G10_PADCFG[2]	3G10_PADCFG[1]	3G10_PADCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP 4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

N14P-GT1-A2	0x0FE4	0010	15K ohm pull-down	0100	25K ohm pull-down
N14P-GV2-B-A1	0x1292	1000	5K ohm pull-up	0010	15K ohm pull-down

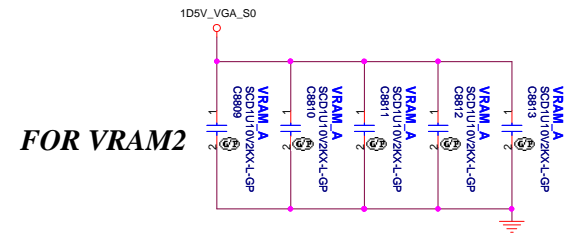
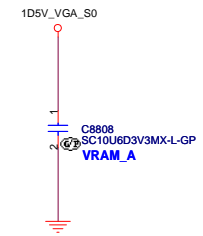
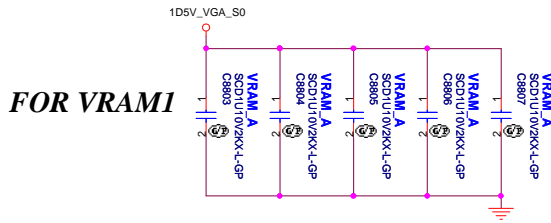
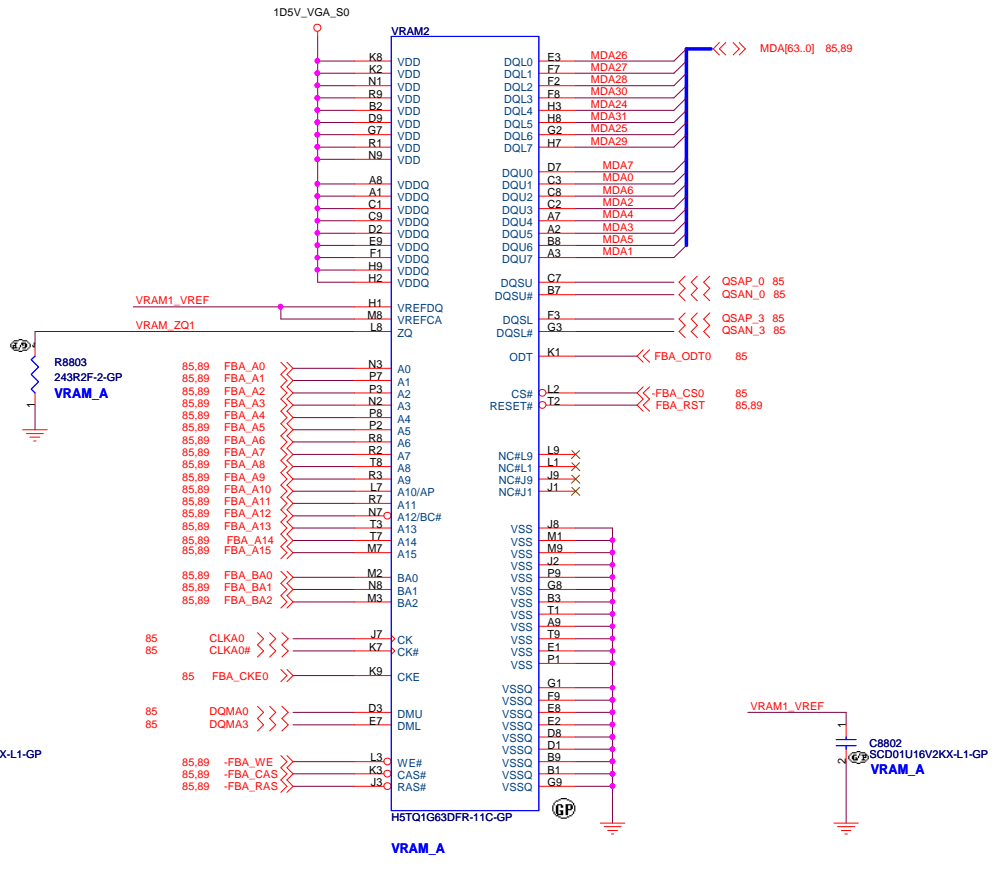
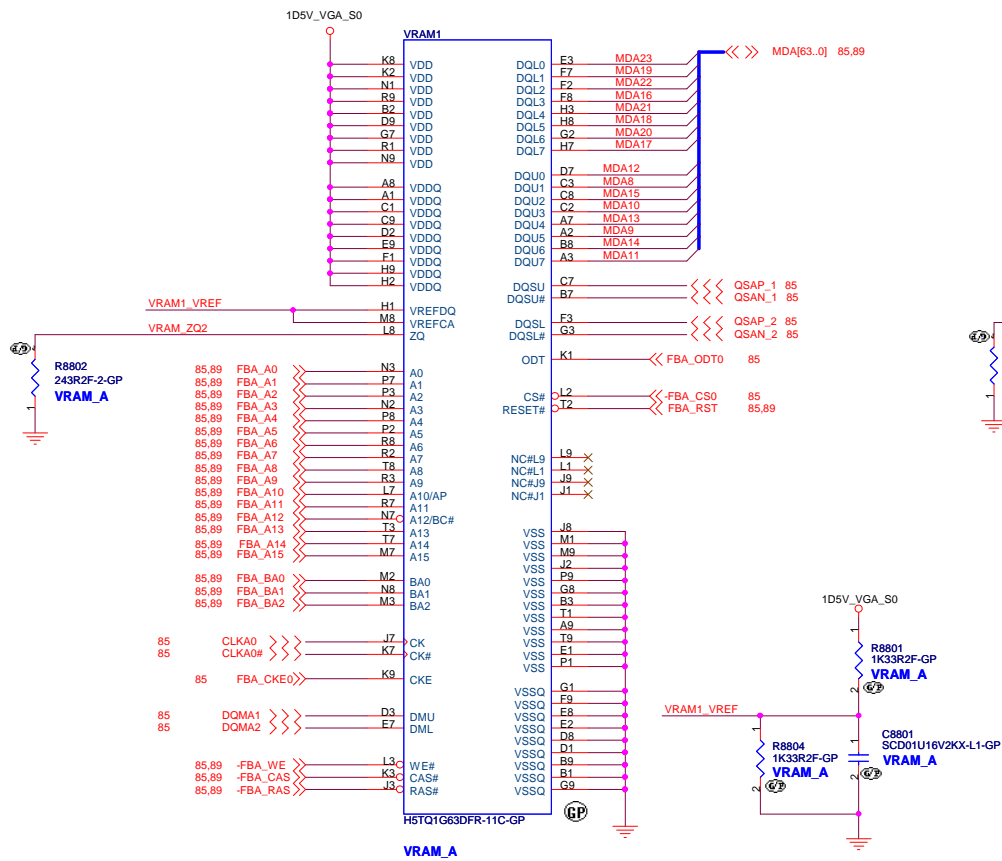




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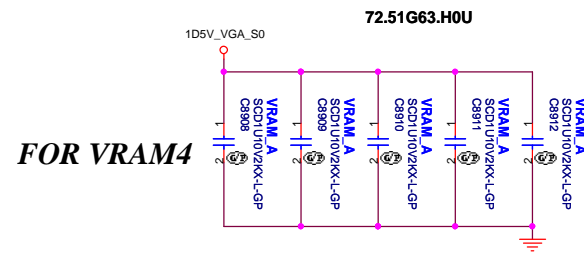
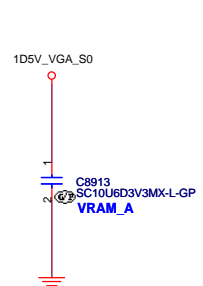
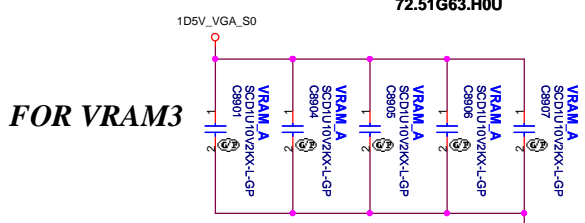
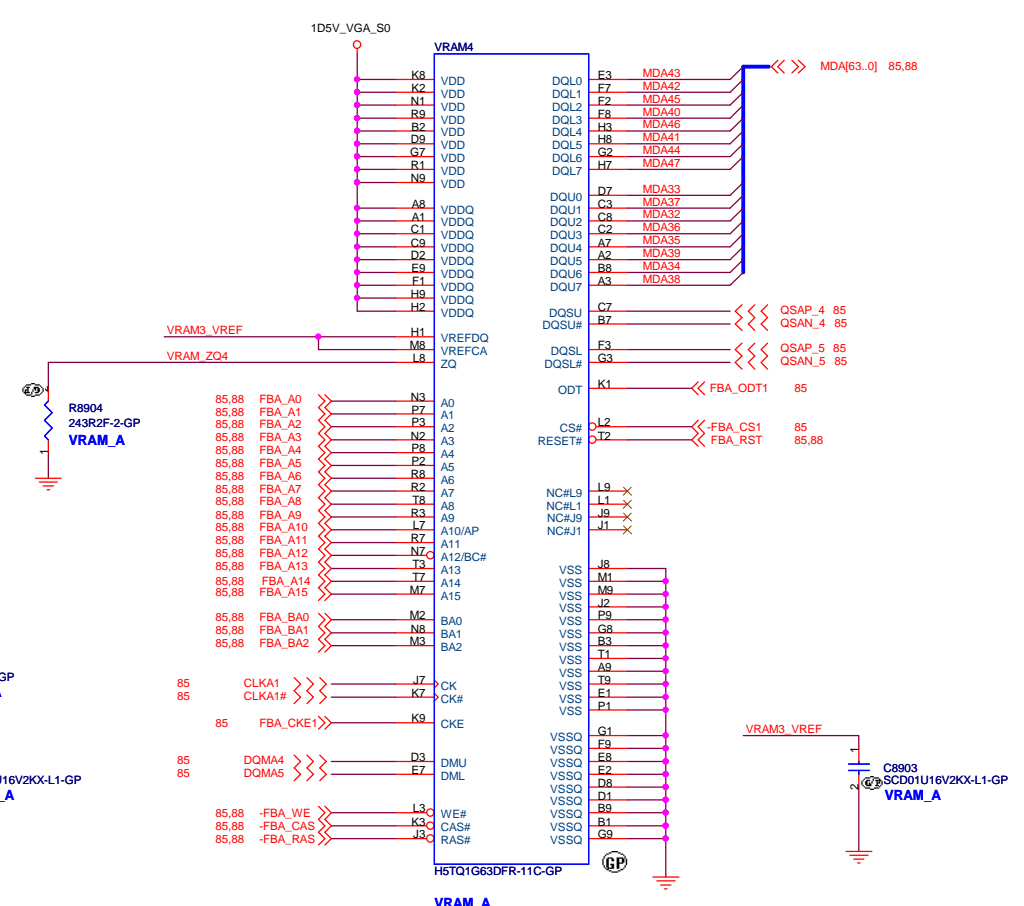
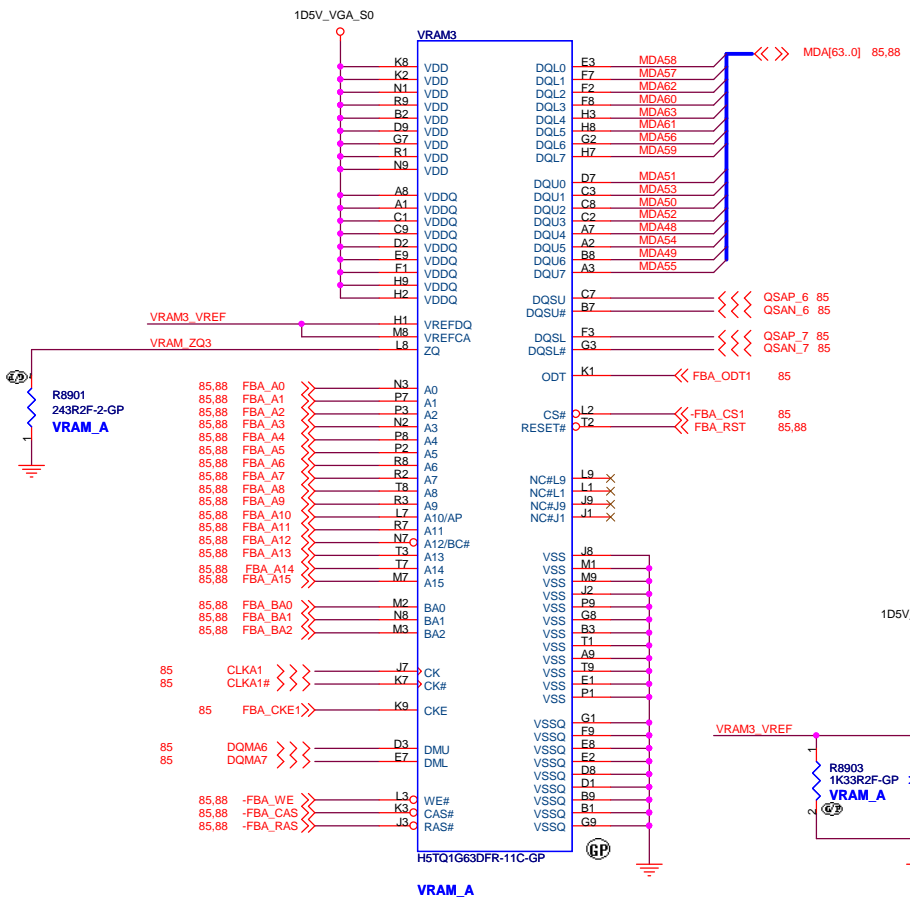
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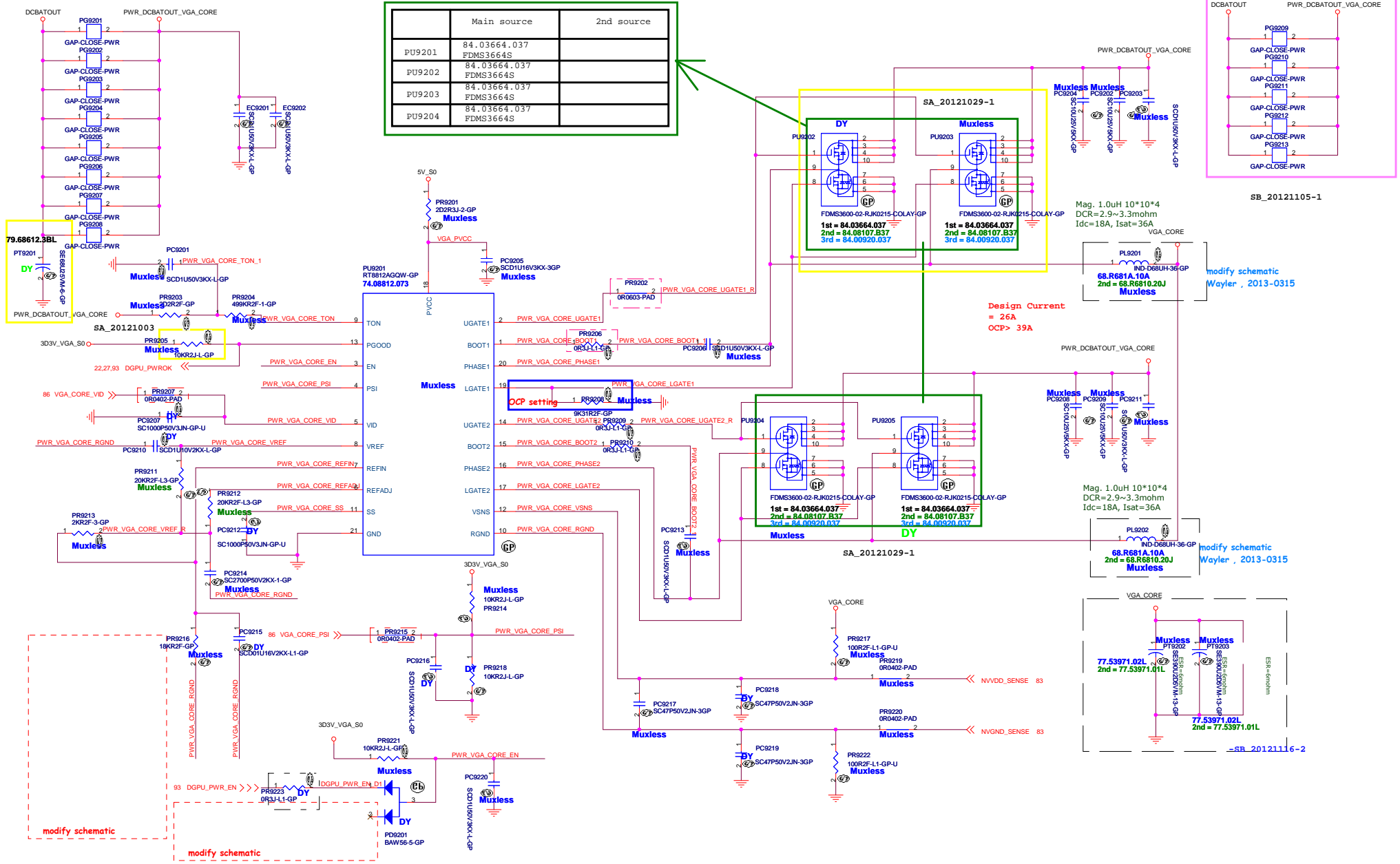
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GPU-VRAM5,6 (3/4)		
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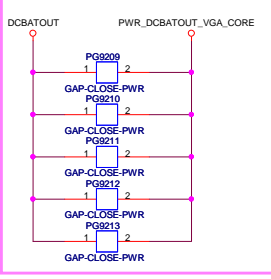
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GPU-VRAM7.8 (4/4)		
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PU9202	84.03664.037 FDM3664S	
PU9203	84.03664.037 FDM3664S	
PU9204	84.03664.037 FDM3664S	



Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Design Current = 26A
OCP > 39A

modify schematic
Wayler, 2013-0315

modify schematic
Wayler, 2013-0315

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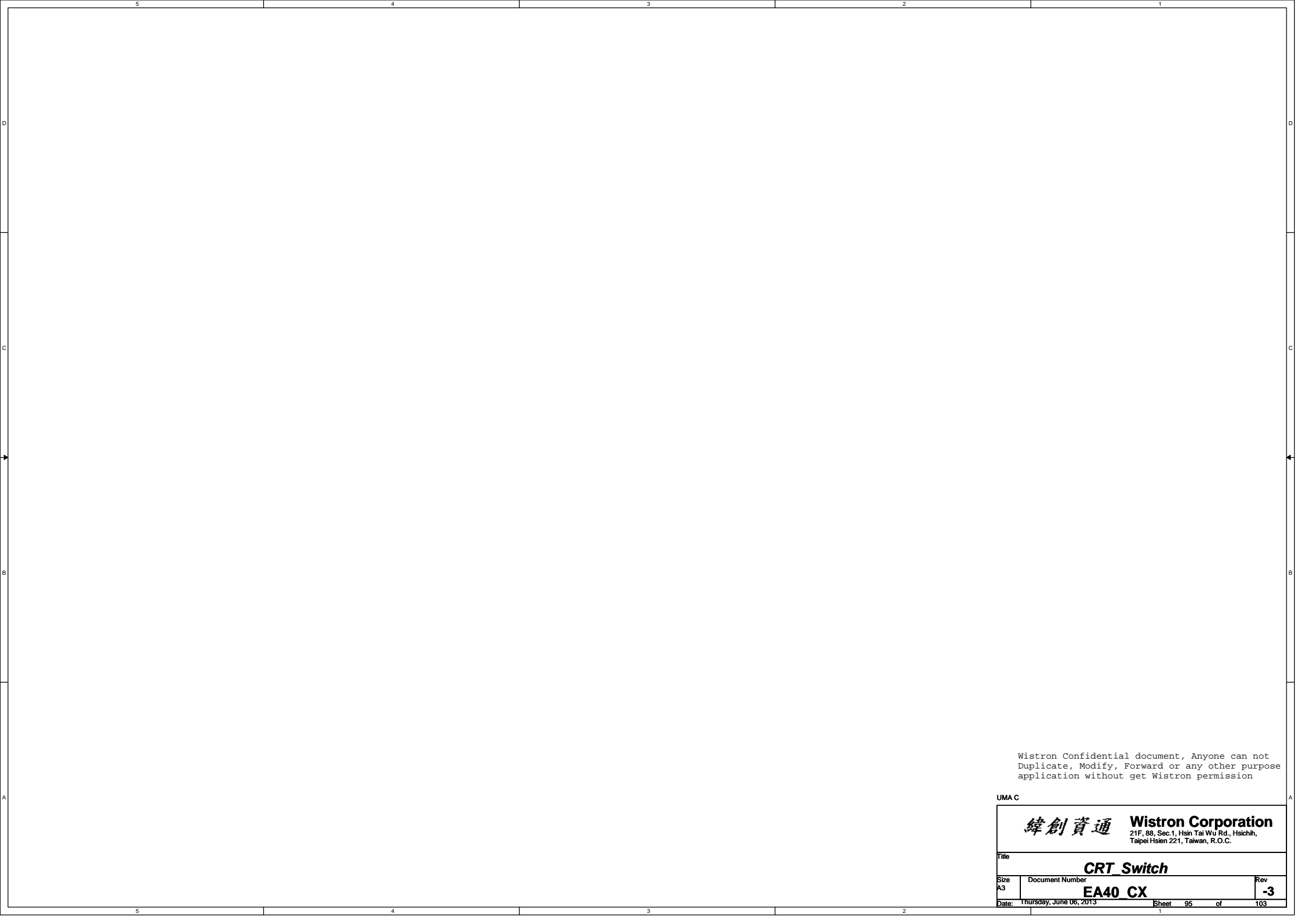
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<p>Title</p> <p>LVDS Switch</p>		
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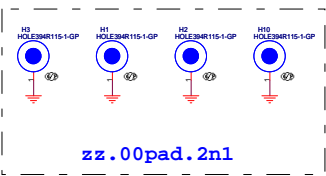
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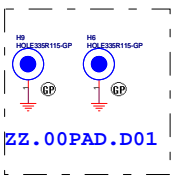
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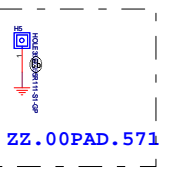
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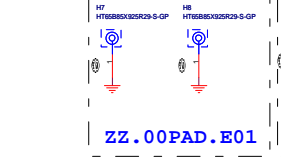
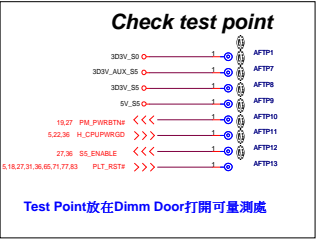
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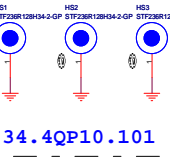
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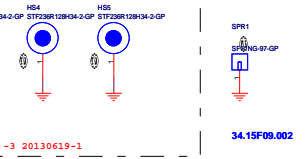
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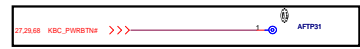
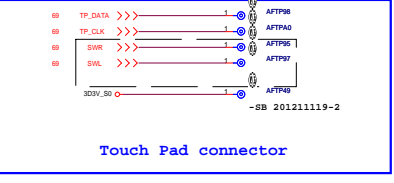
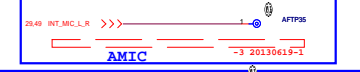
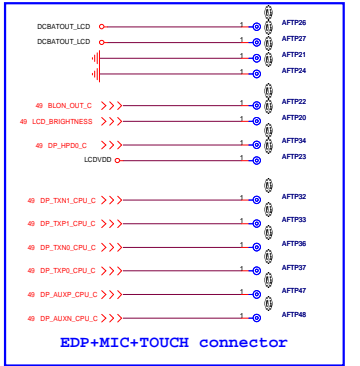
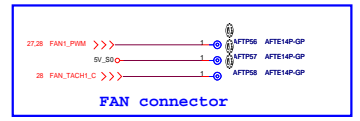
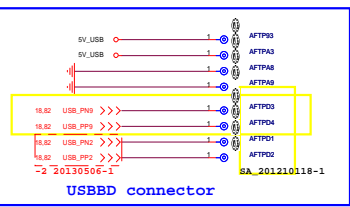
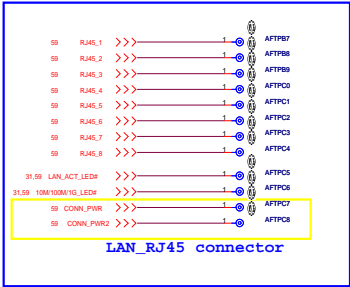
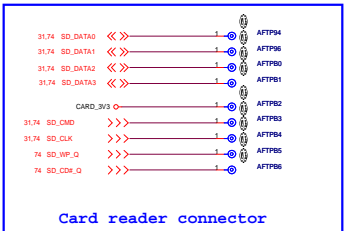
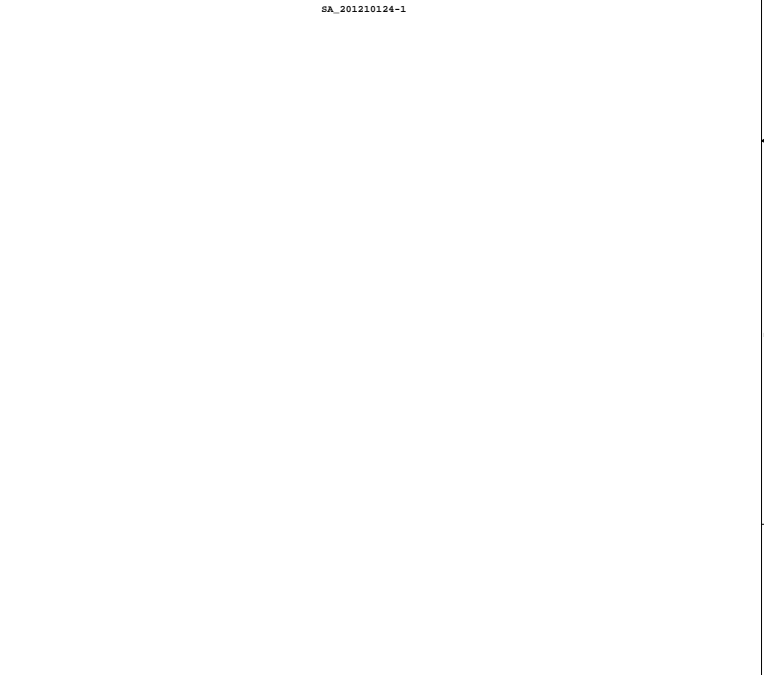
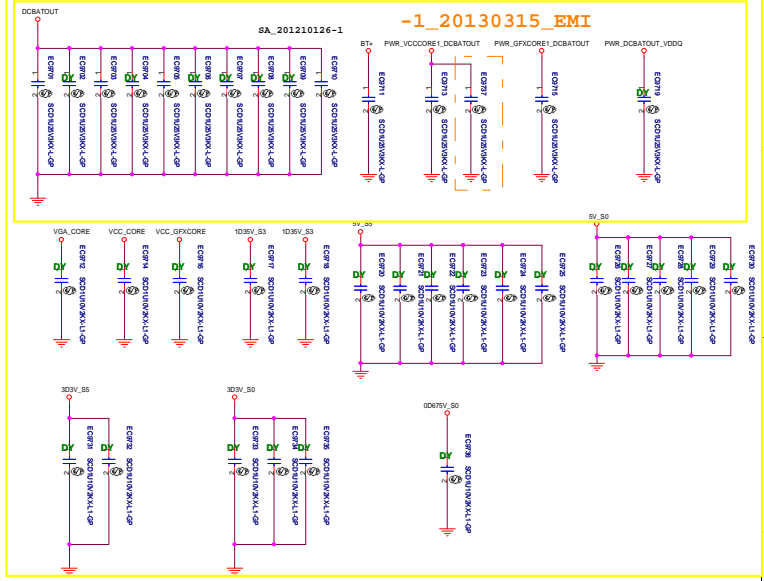
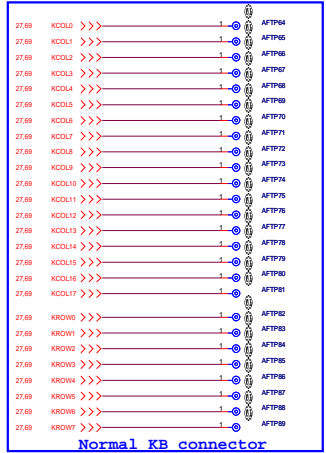
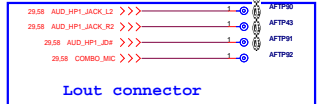
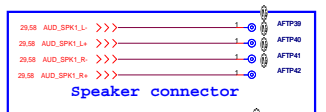
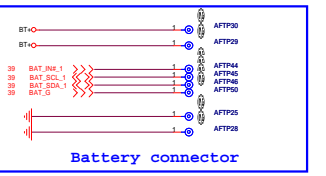
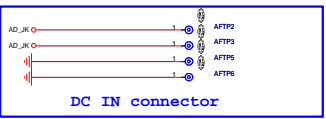
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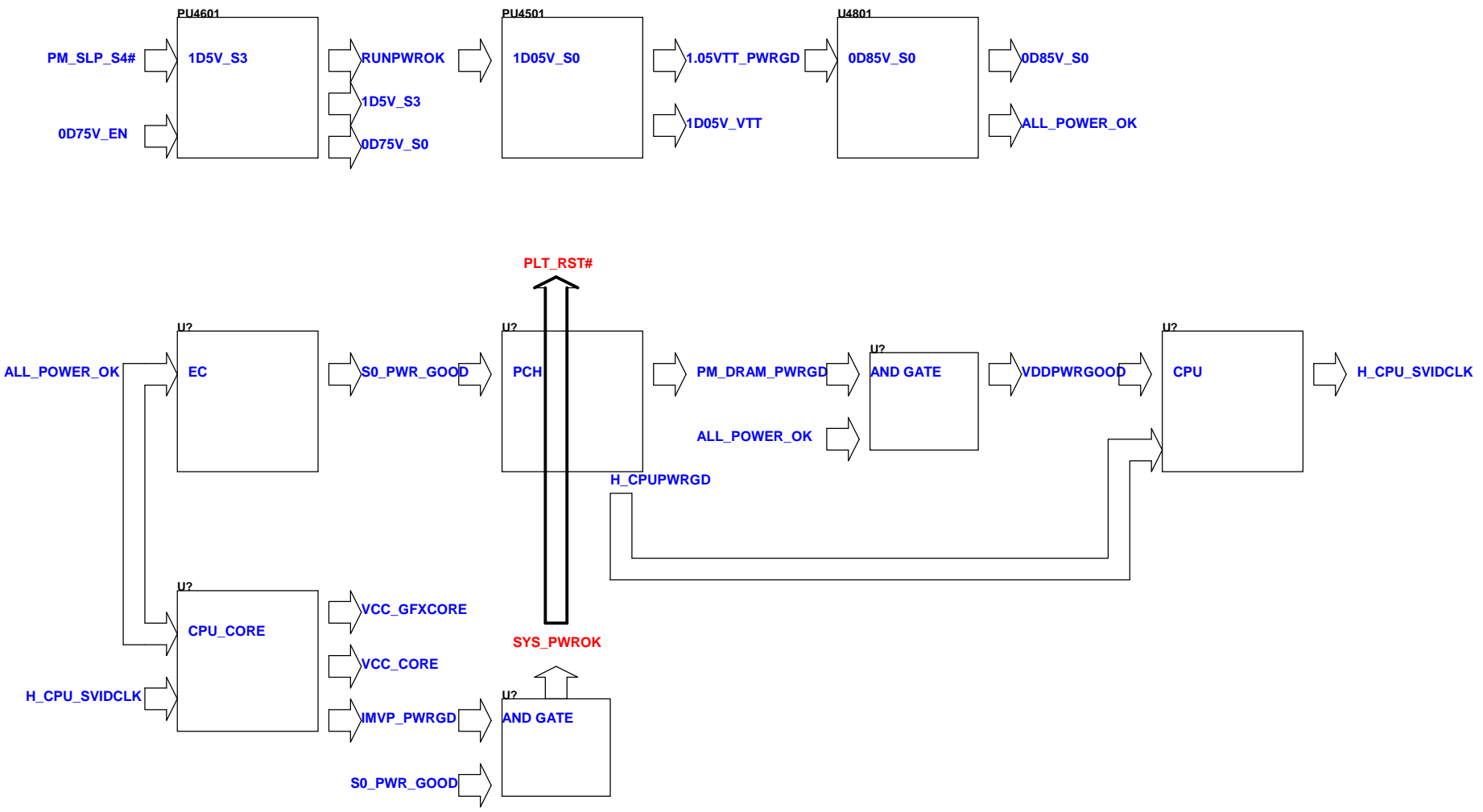


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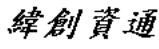


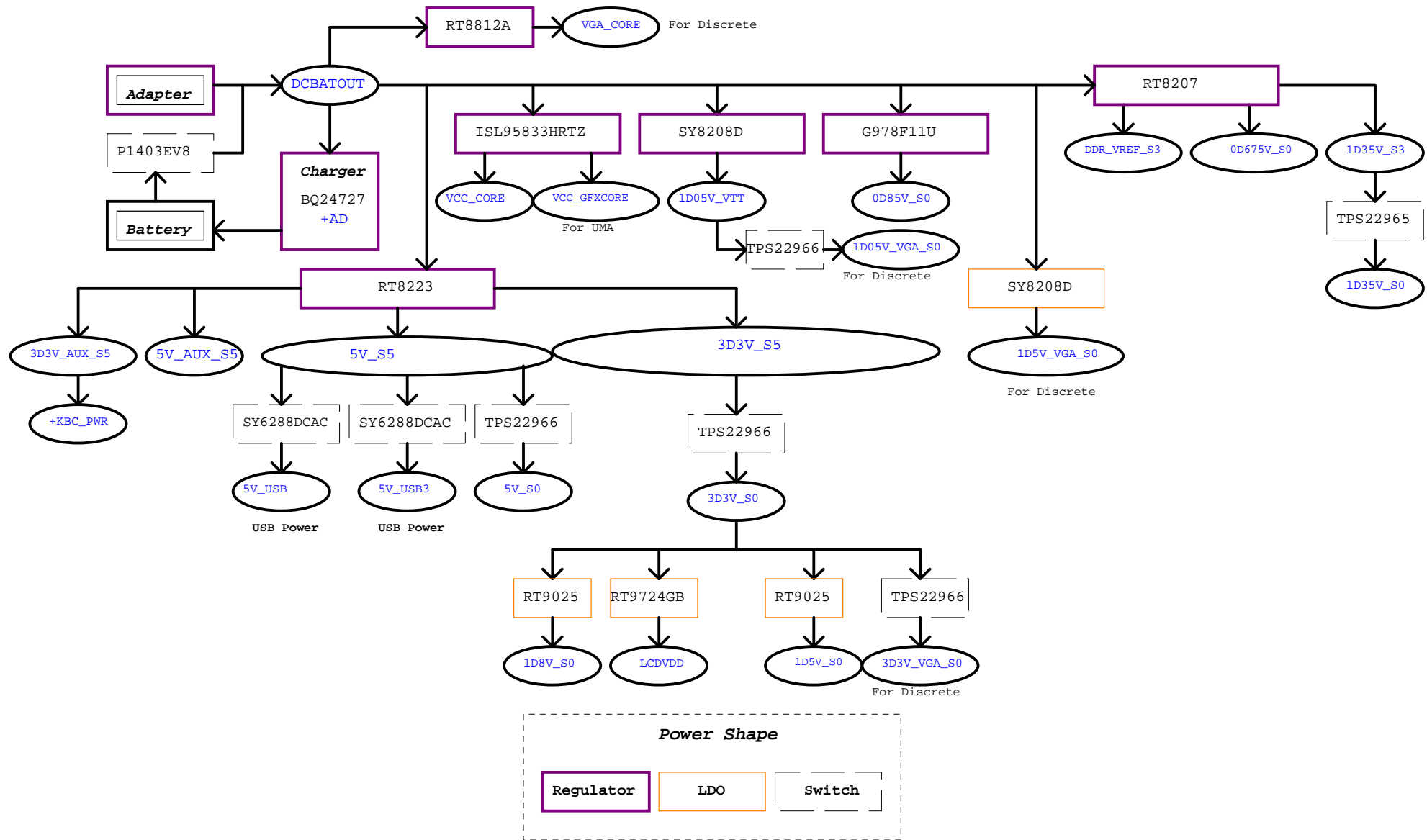
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Power Sequence



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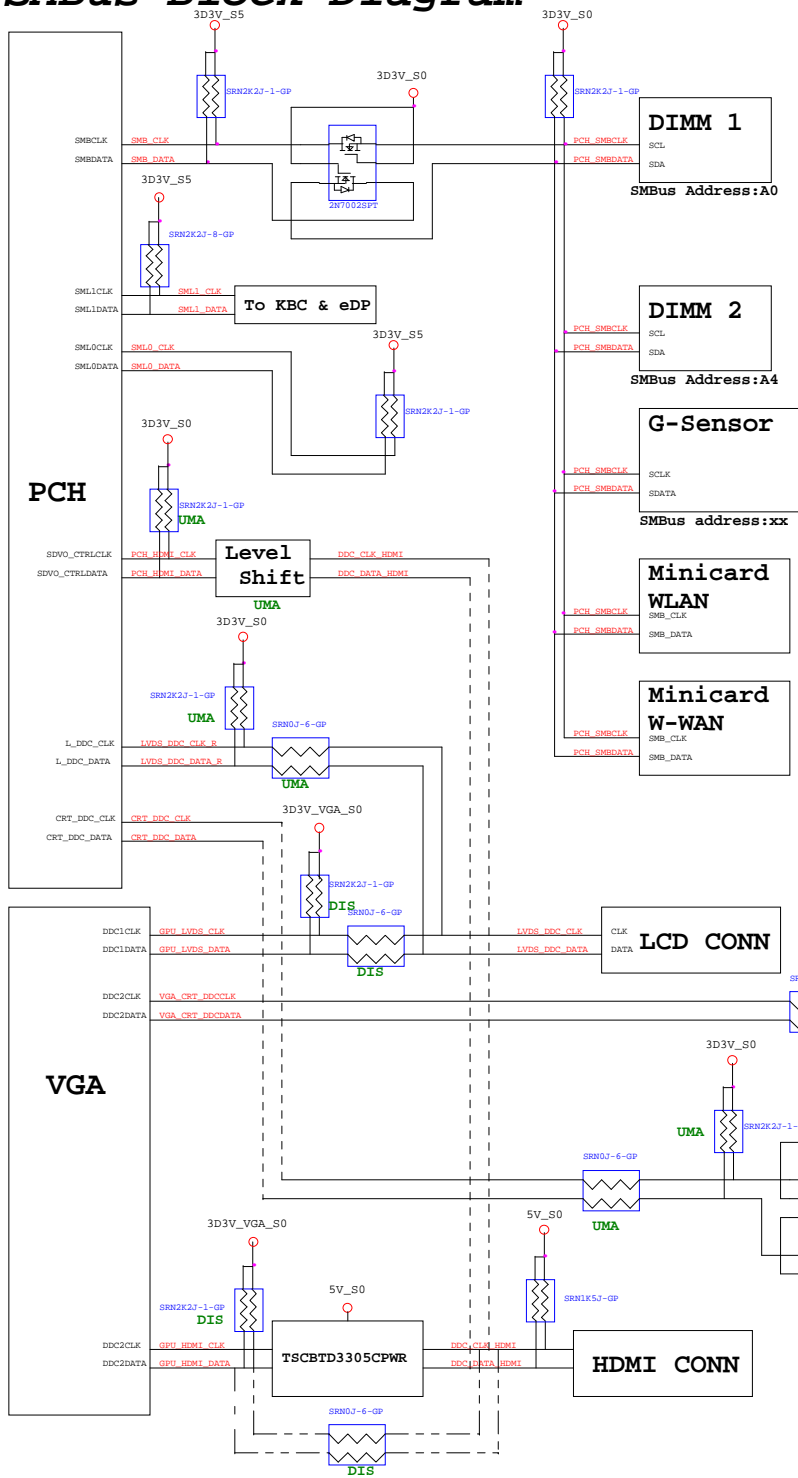


Power Shape

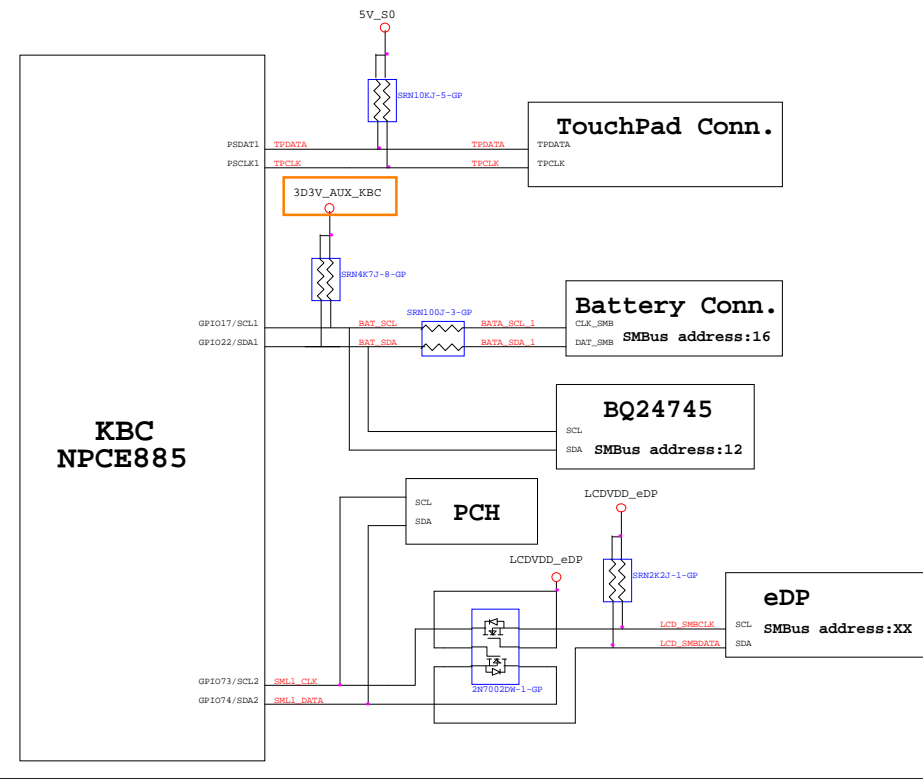


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PCH SMBus Block Diagram



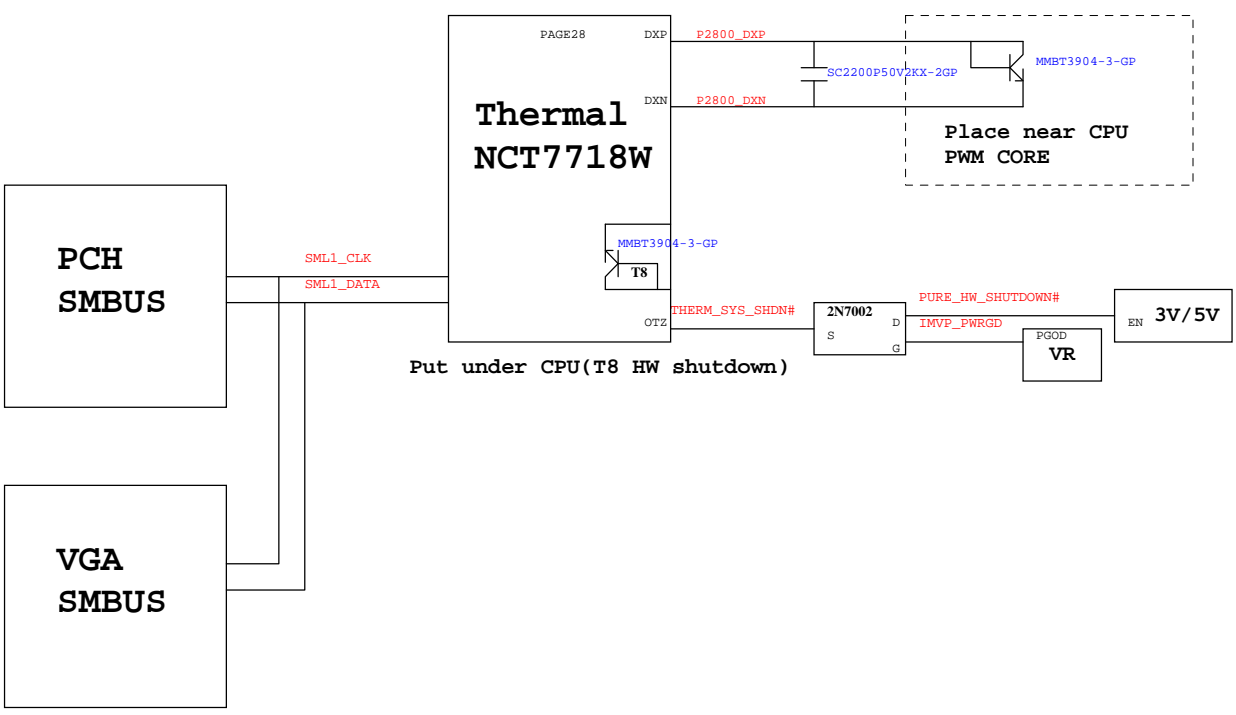
KBC SMBus Block Diagram



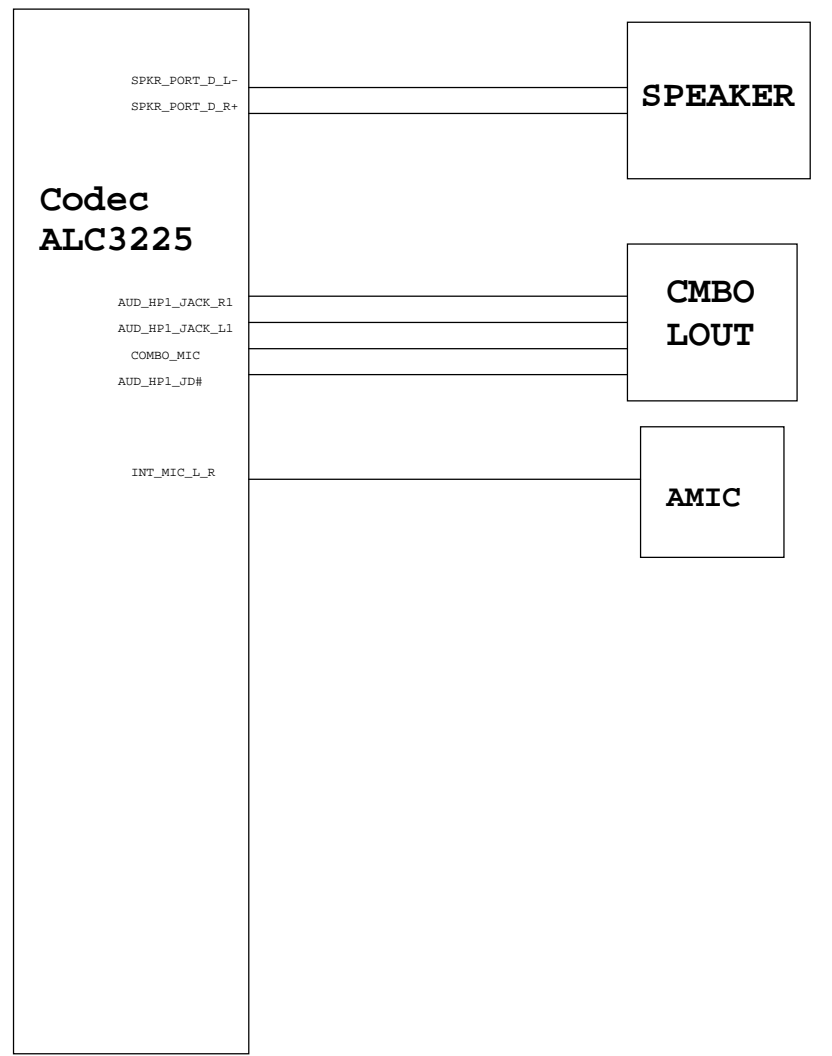
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Thermal Block Diagram



Audio Block Diagram



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