

# Yukon Block Diagram

Project code: 91.4BC01.001  
 PCB P/N : 48.4BC01.001  
 REVISION : 08226- -1

**PCB Layer Stackup**

L1: Signal 1  
 L2: VCC  
 L3: Inner Signal 2  
 L4: Inner Signal 3  
 L5: GND  
 L6: Signal 4

**CPU V\_CORE**

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

**SYSTEM DC/DC**

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID8V_S3

**SYSTEM DC/DC**

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

**SYSTEM LDO**

INPUT	OUTPUT
1D8V_S3	0D9V_S3

**SYSTEM LDO**

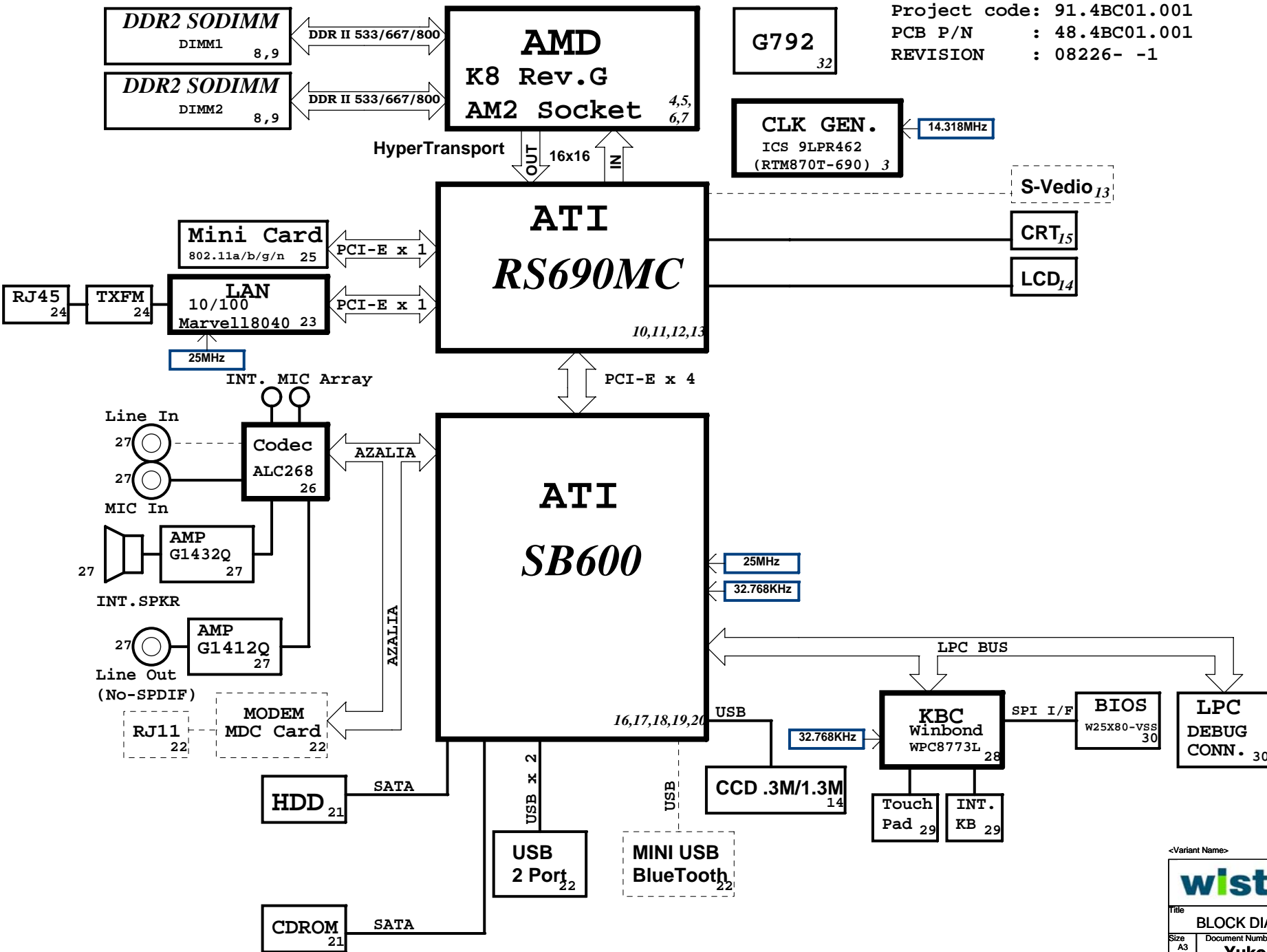
INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

**SYSTEM LDO**

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

**Battery Charger**

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT



<Variant Name>

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 Hsichih, Taipei

Title: **BLOCK DIAGRAM**

Size A3	Document Number	Rev
	<b>Yukon</b>	-1
Date: Tuesday, August 12, 2008	Sheet 1 of 43	

5

4

3

2

1

D

D

C

C

B

B

A

A

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title **CHANGE HISTORY**

Size A3	Document Number <b>Yukon</b>	Rev 1
Date: Wednesday, August 06, 2008	Sheet 2 of	43

5

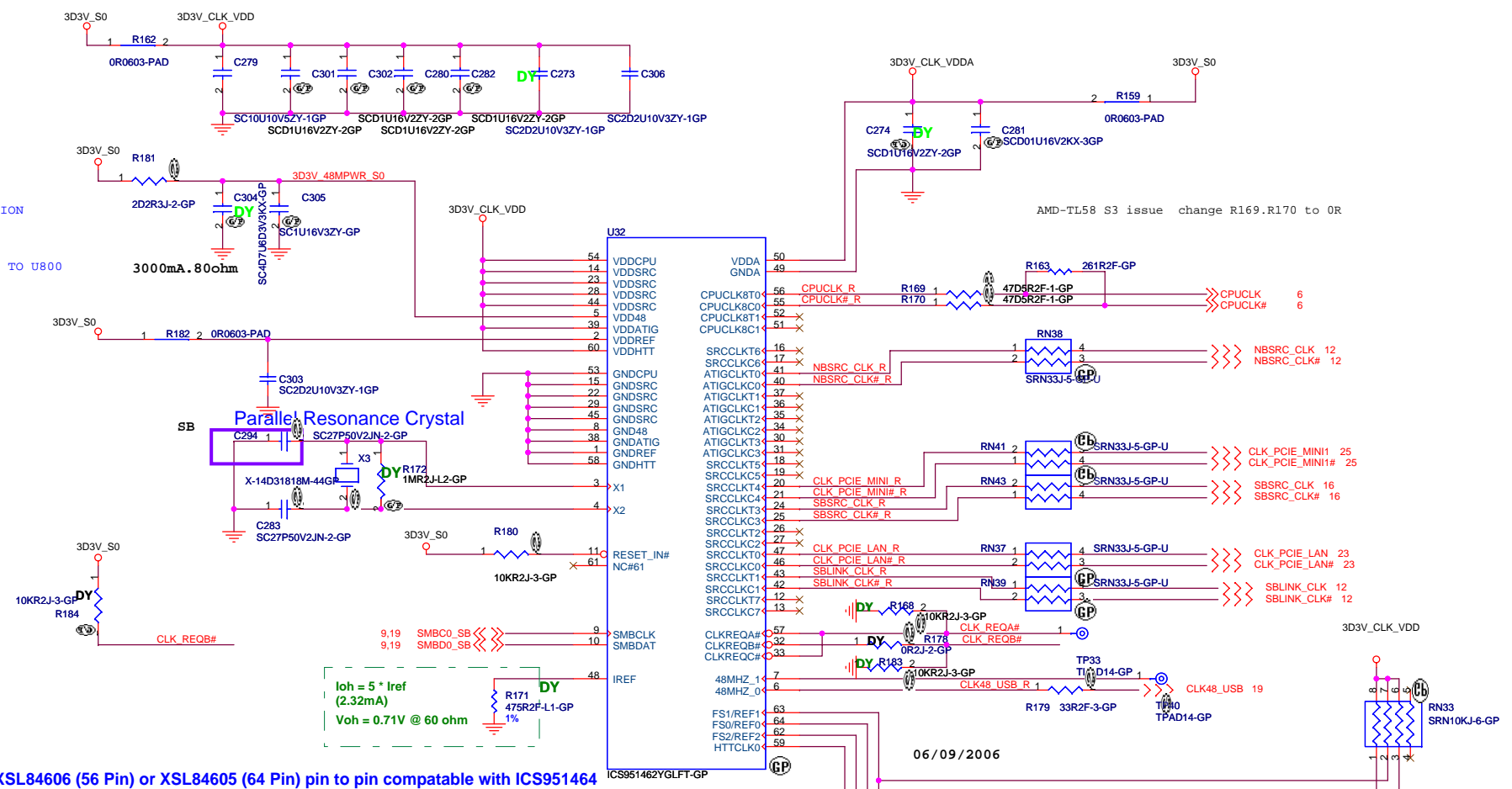
4

3

2

1

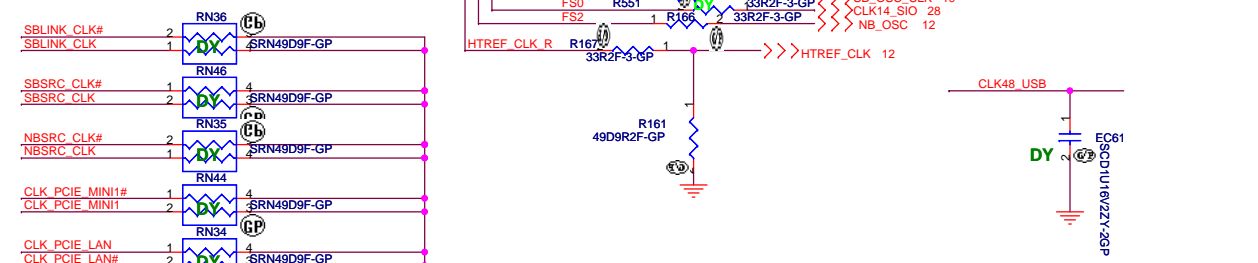
- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Check SLGO EXT CLK XSL84606 (56 Pin) or XSL84605 (64 Pin) pin to pin compatible with ICS951464

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operator



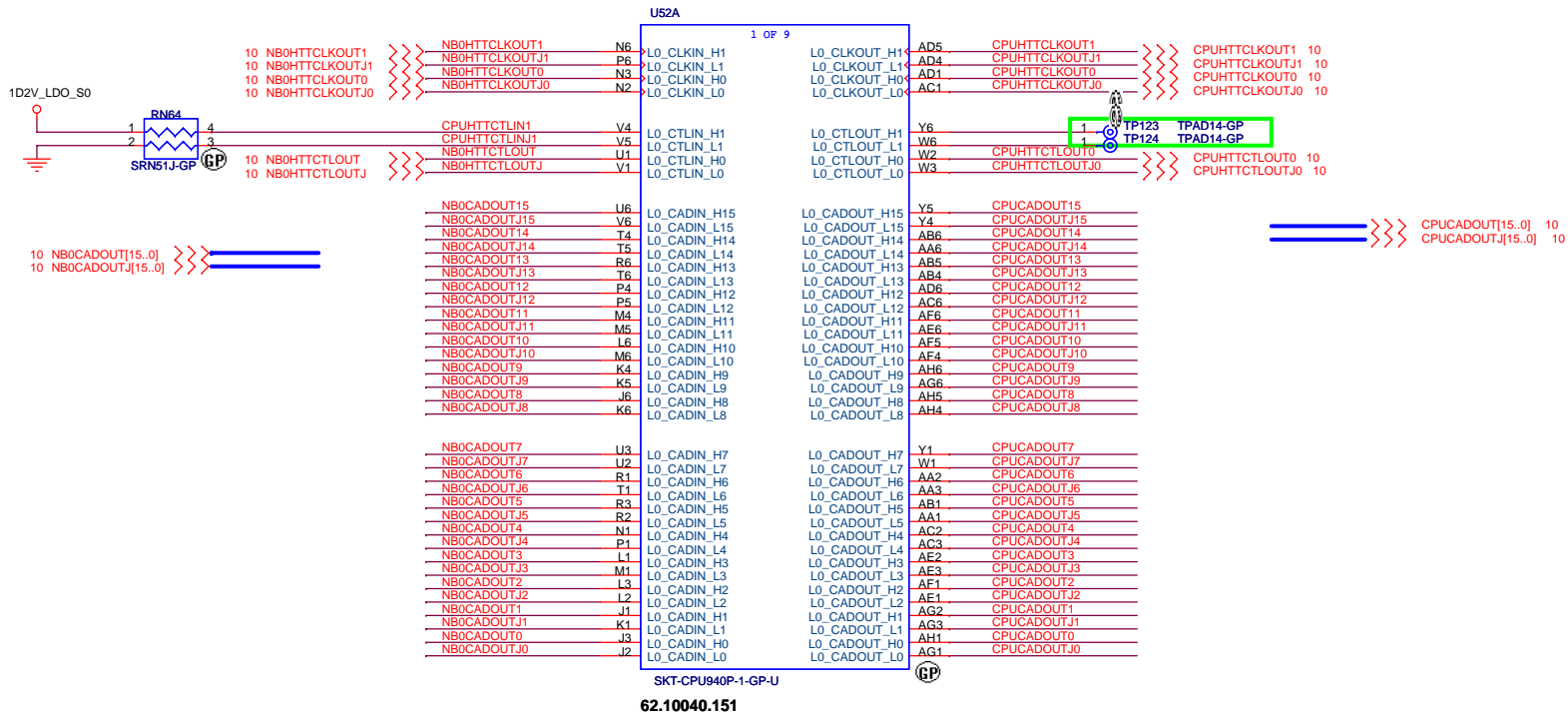
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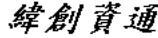
Title: **CLKGEN\_ICS951412**

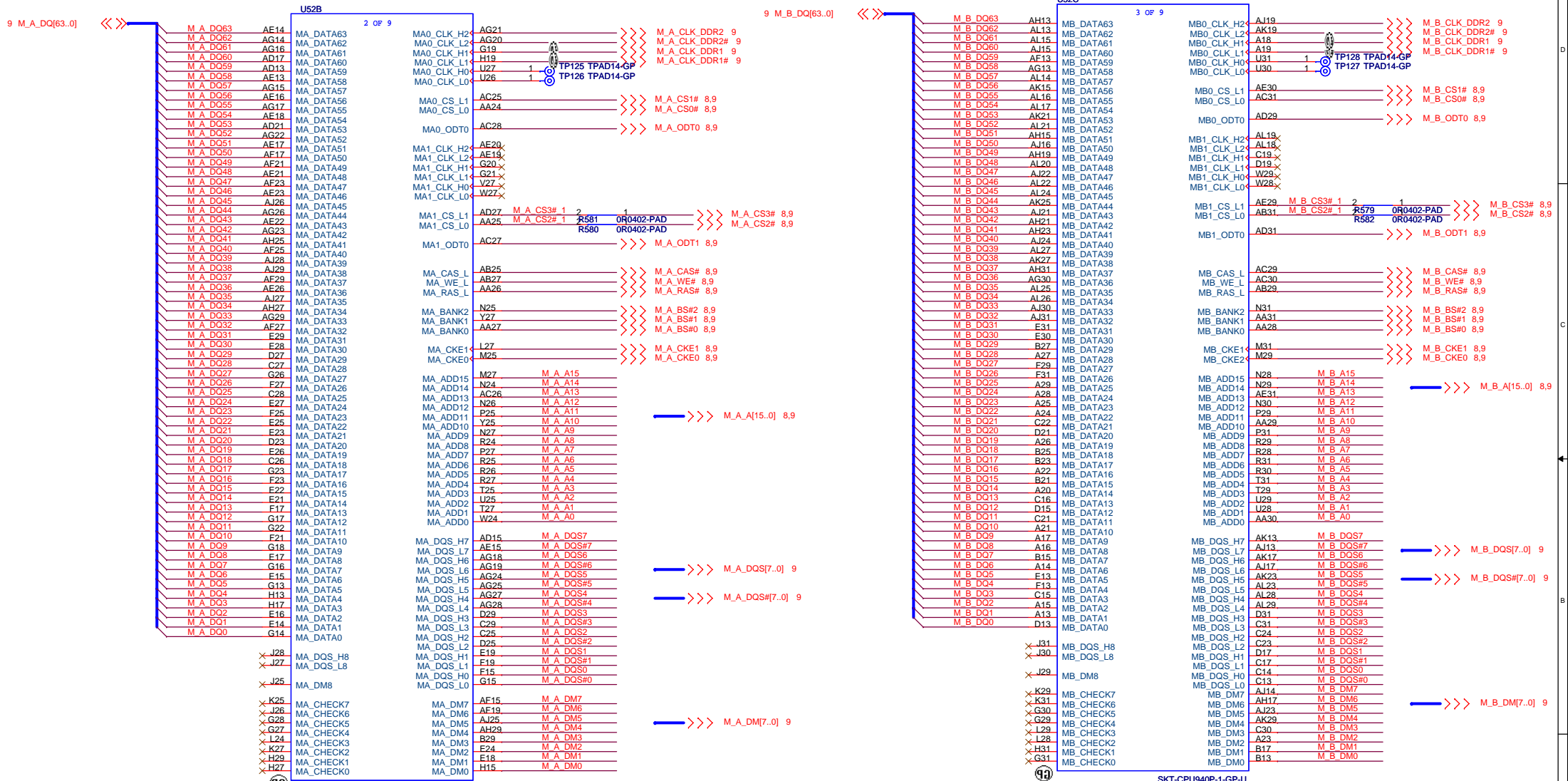
Size: A3 Document Number: **Yukon** Rev: -1

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<b>Yukon</b>		
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62.10040.151 SKT-CPU940P-1-GP-U

62.10040.151 SKT-CPU940P-1-GP-U

<Core Design>

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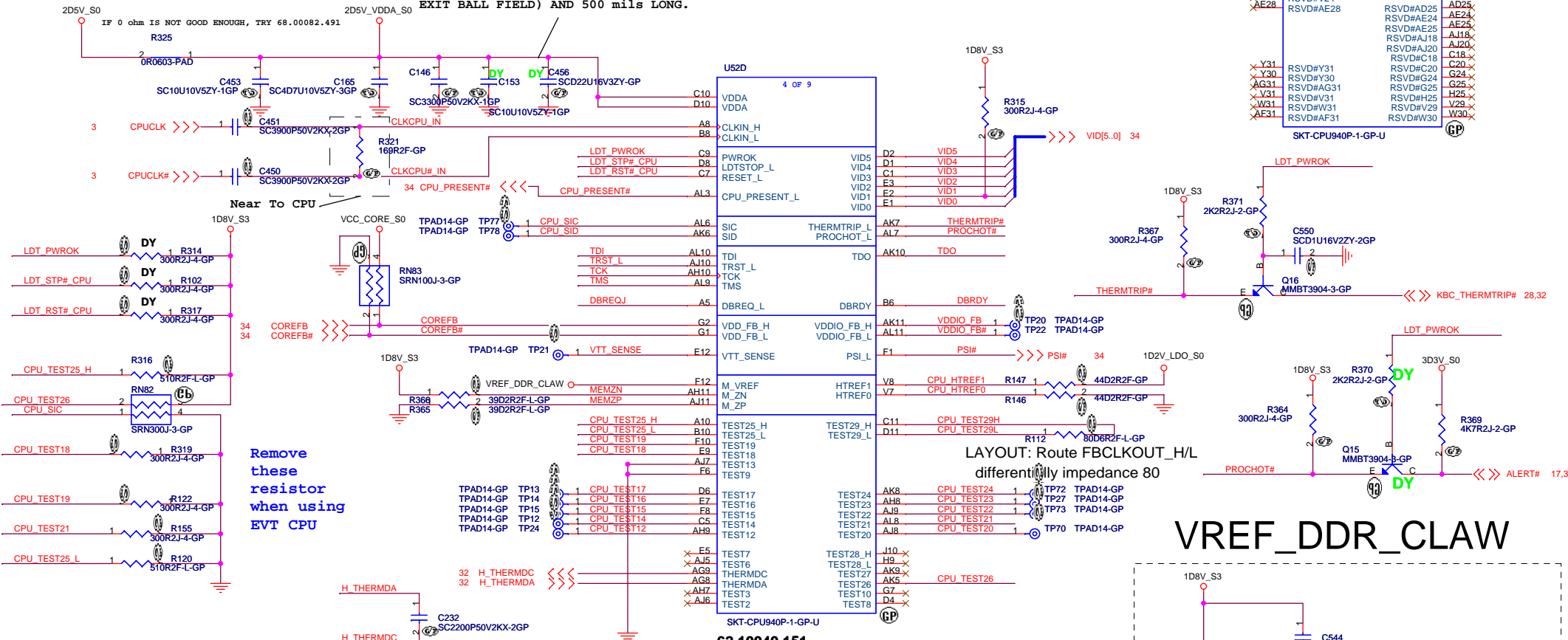
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Title: **CPU(2/4) DDR**

Size: A3 Document Number: **Yukon** Rev: -1

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LYAOUT:ROUTE VDDA TRACE APPROX.  
50mils WIDE(USE 2X25 mil TRACES TO  
EXIT BALL FIELD) AND 500 mils LONG.

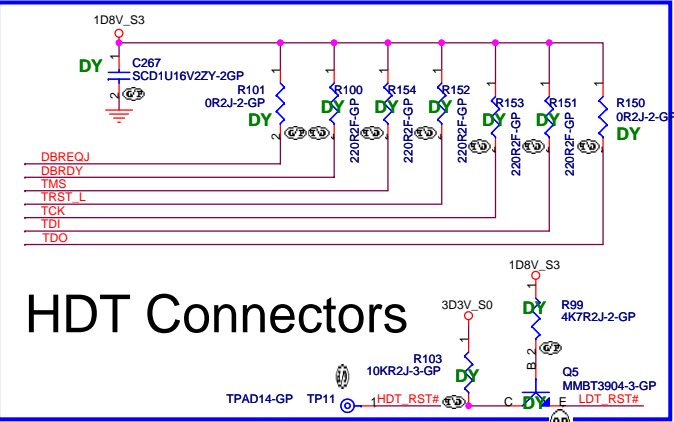
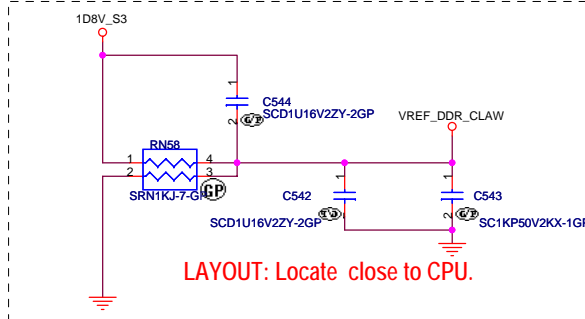


Near To CPU

Remove these resistor when using EVT CPU

LAYOUT: Route FBCLKOUT\_H/L differentially impedance 80

VREF\_DDR\_CLAW



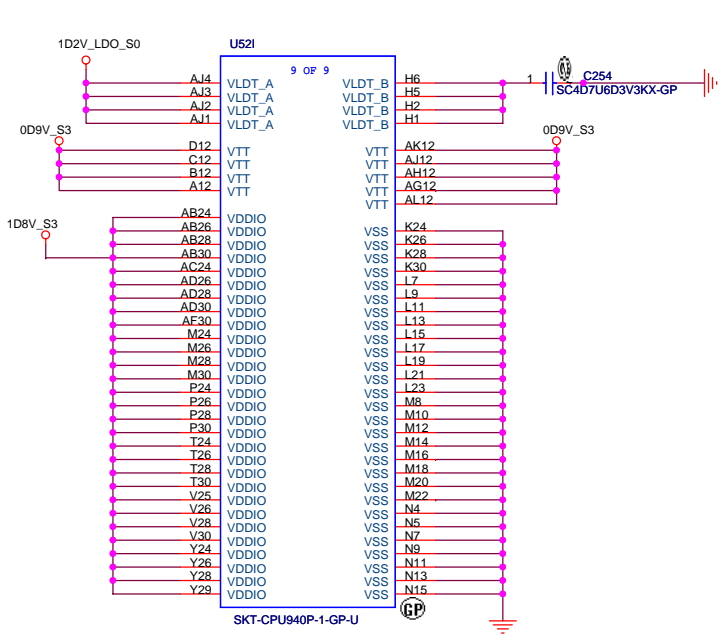
<Core Design>

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Title: **CPU(3/4)\_Control & Debug**

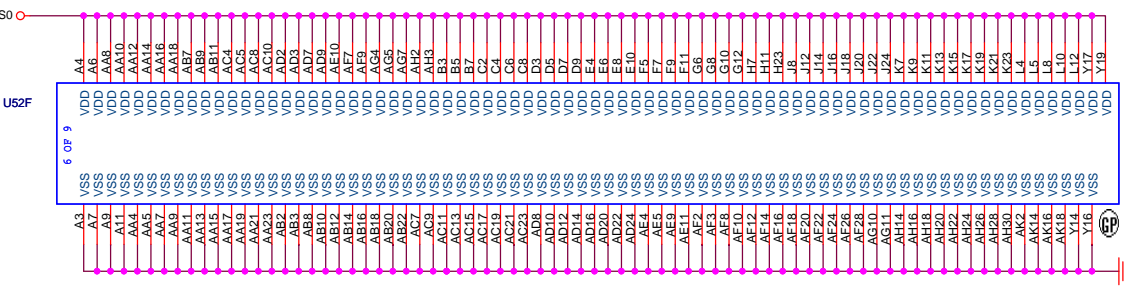
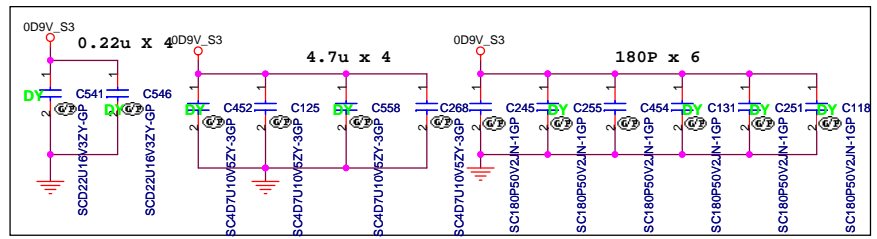
Size: A3 Document Number: **Yukon** Rev: -1

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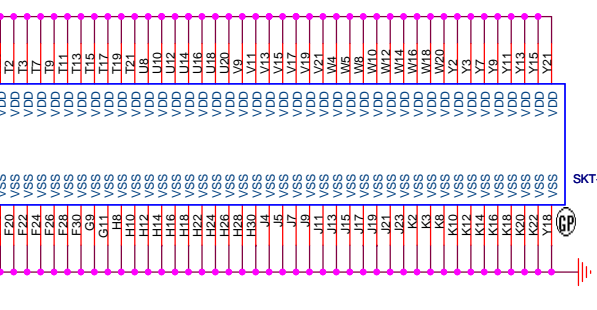
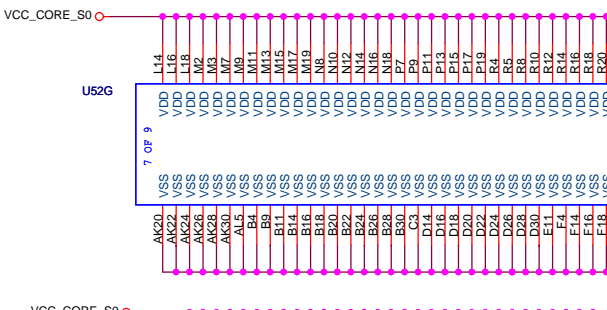


62.10040.151

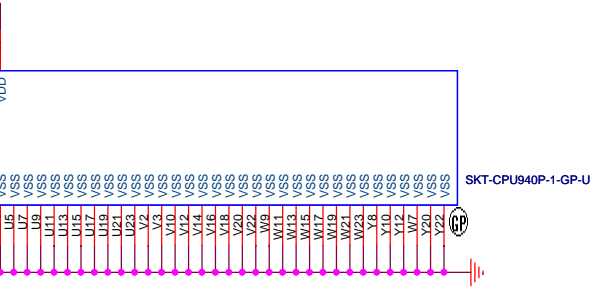
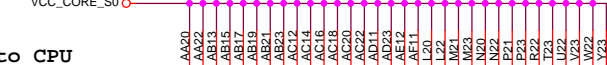
Place near to CPU



SKT-CPU940P-1-GP-U

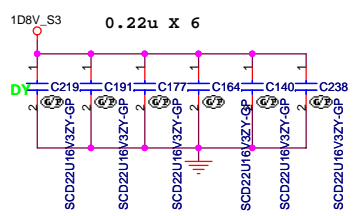
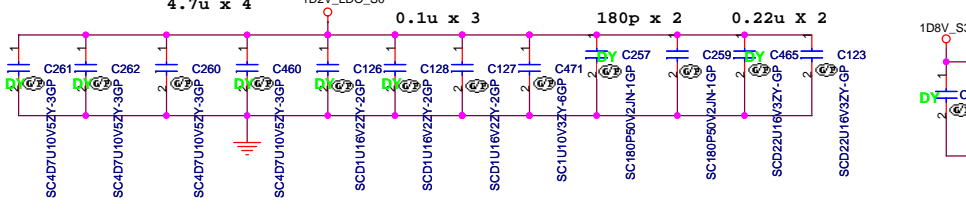
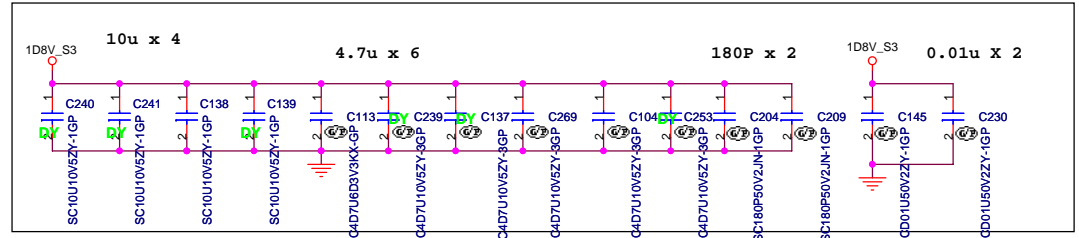
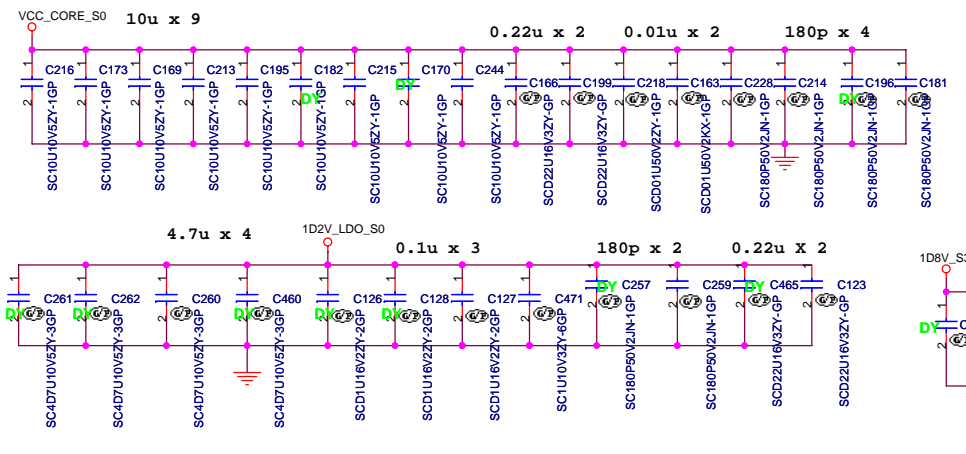


SKT-CPU940P-1-GP-U



SKT-CPU940P-1-GP-U

LAYOUT: Place on backside of processor.

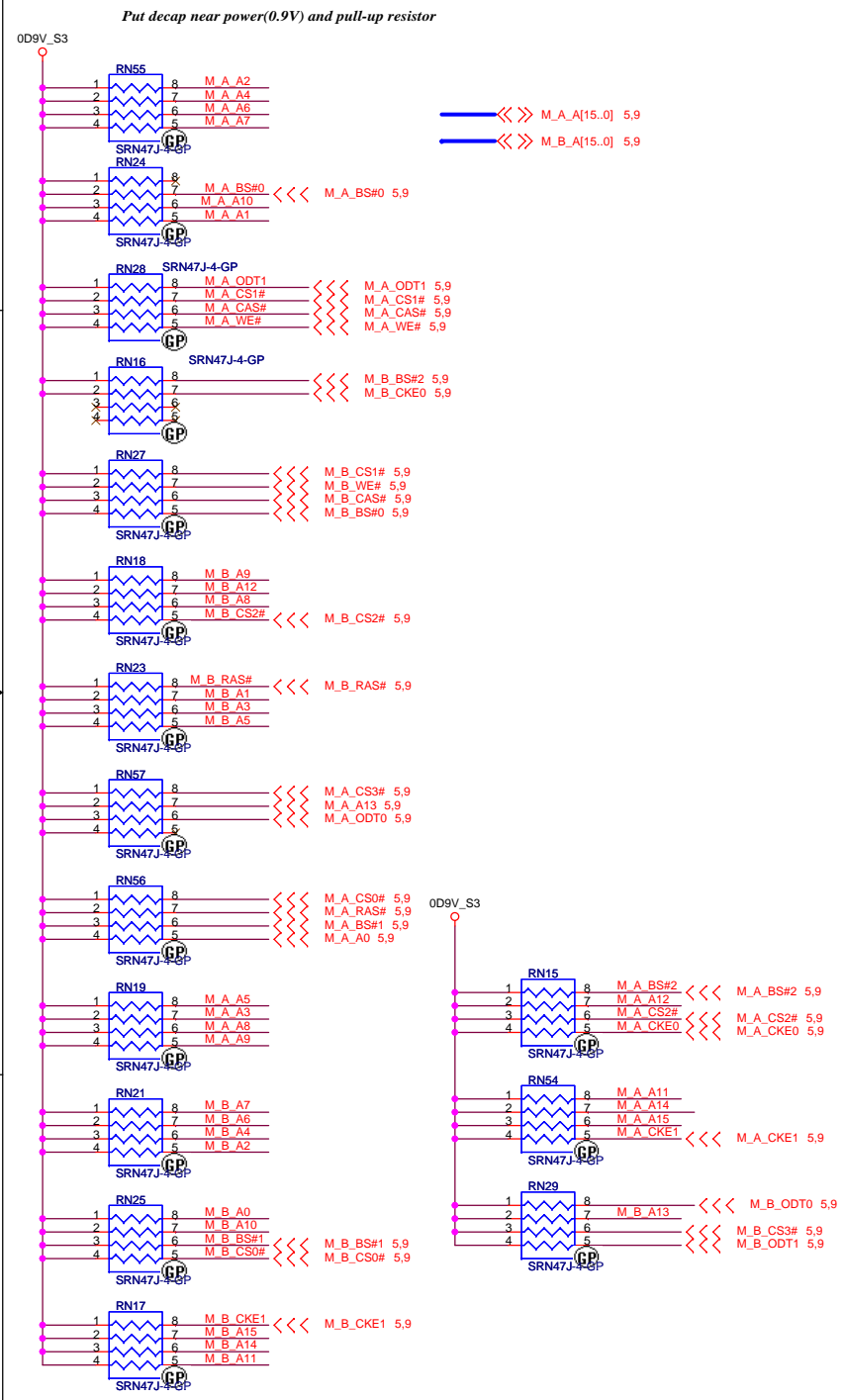


<Core Design>

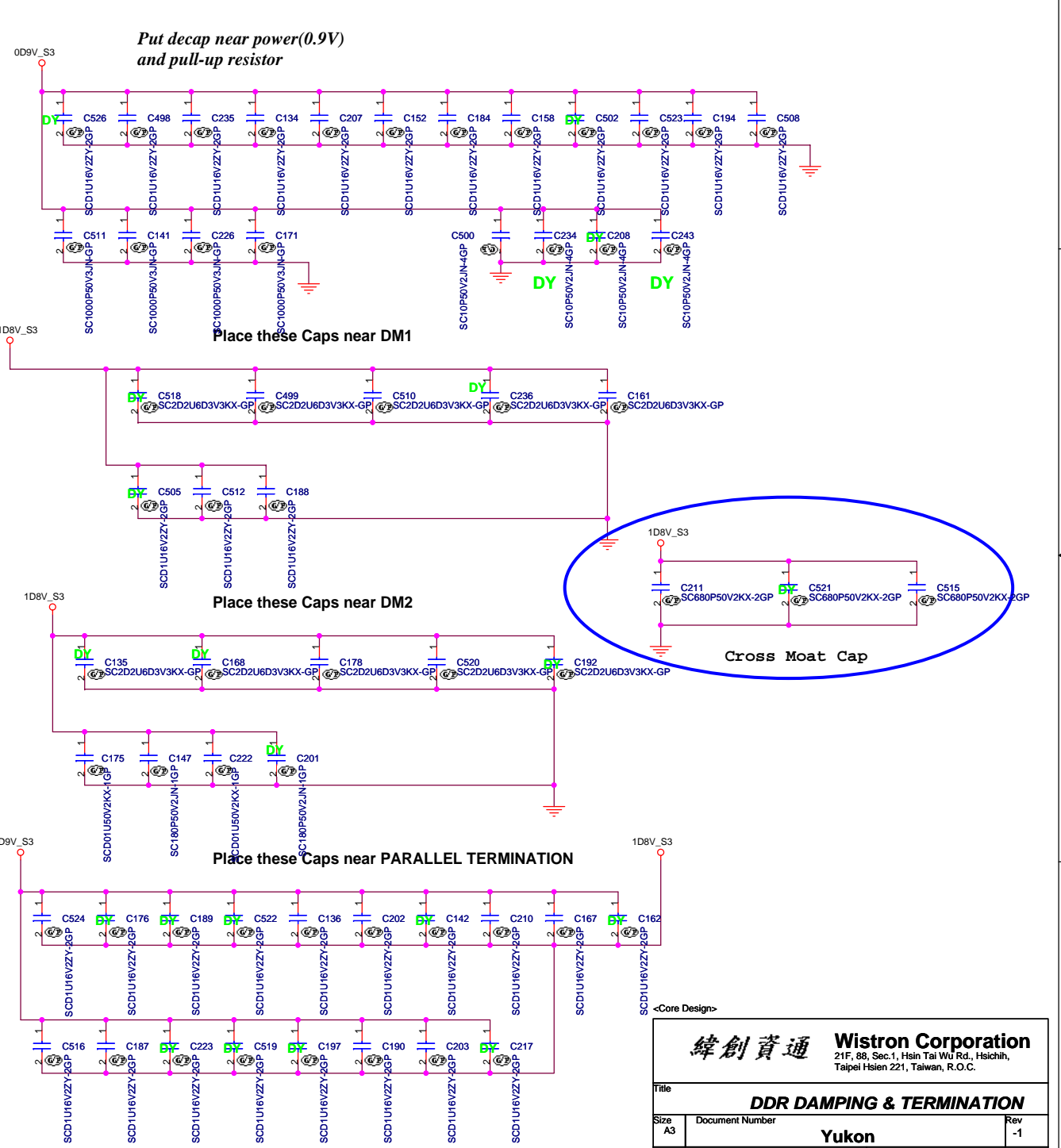
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Title		
<b>CPU(4/4)_Power</b>		
Size	Document Number	Rev
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# PARALLEL TERMINATION



# Decoupling Capacitor

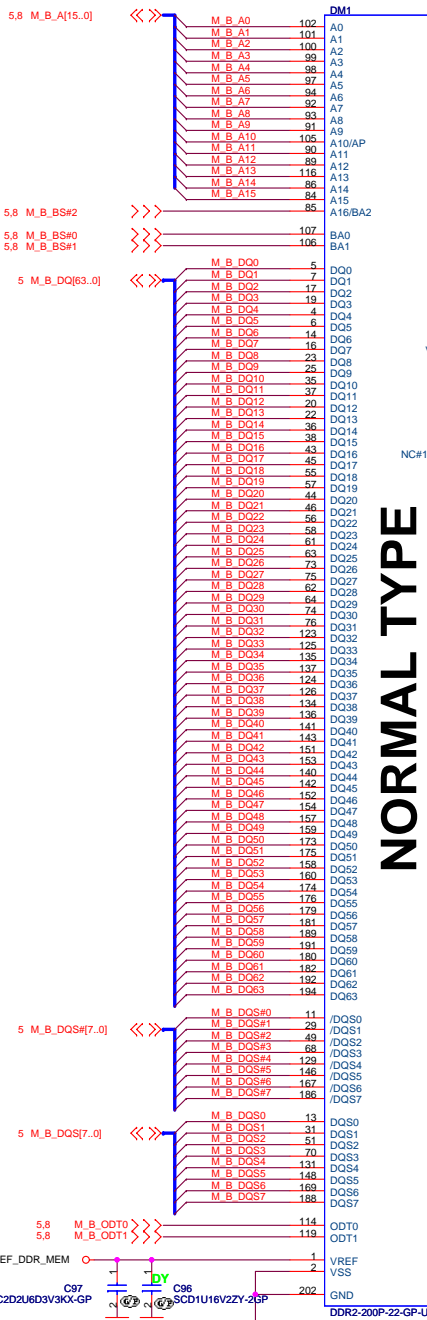


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Title: **DDR DAMPING & TERMINATION**

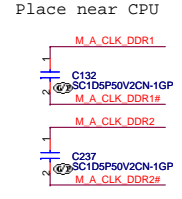
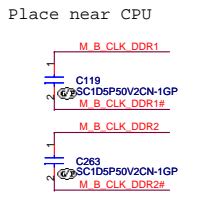
Size A3	Document Number	Rev -1
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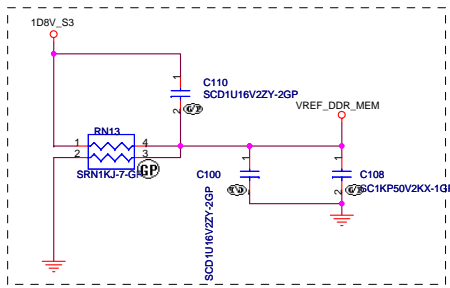


**NORMAL TYPE**

**NORMAL TYPE**



**DDR\_VREF**



LAYOUT: Locate close to DIMM

62.10017.A61  
High 9.2mm  
2nd: 62.10017.A51

62.10017.661  
High 5.2mm  
2nd: 62.10017.A41

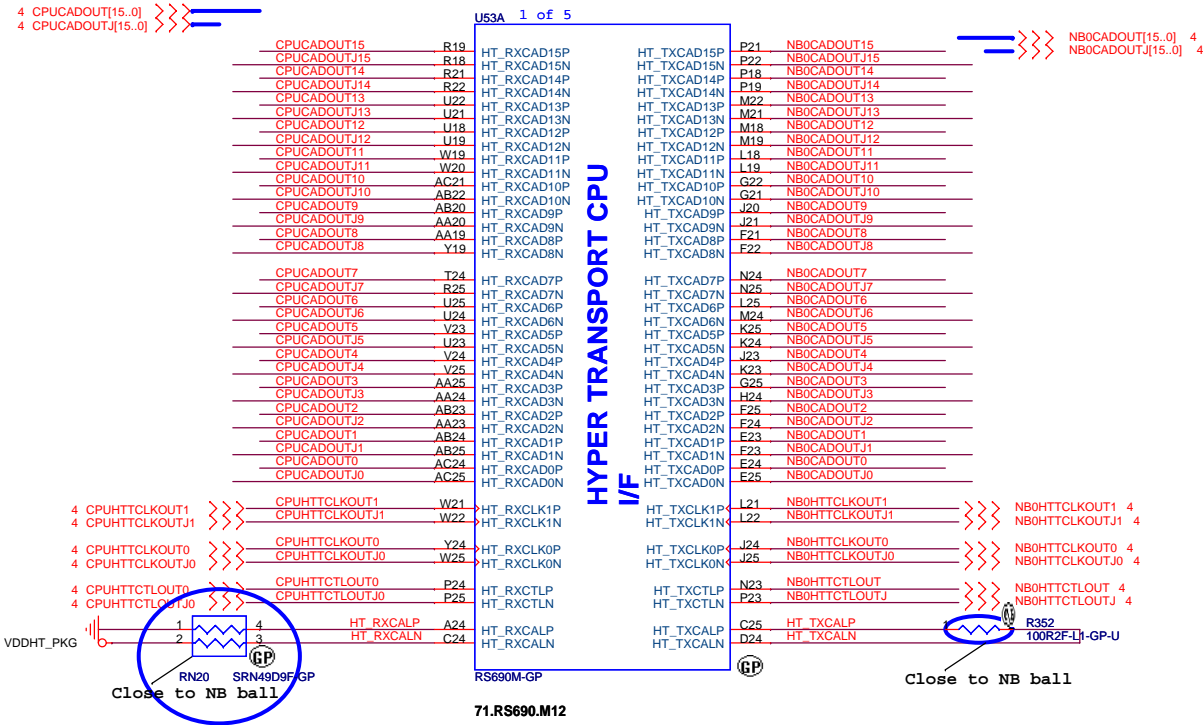
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Title		<b>DDR SO-DIMM SKT</b>	
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# CLAW HAMMER TO NB

# NB TO CLAW HAMMER

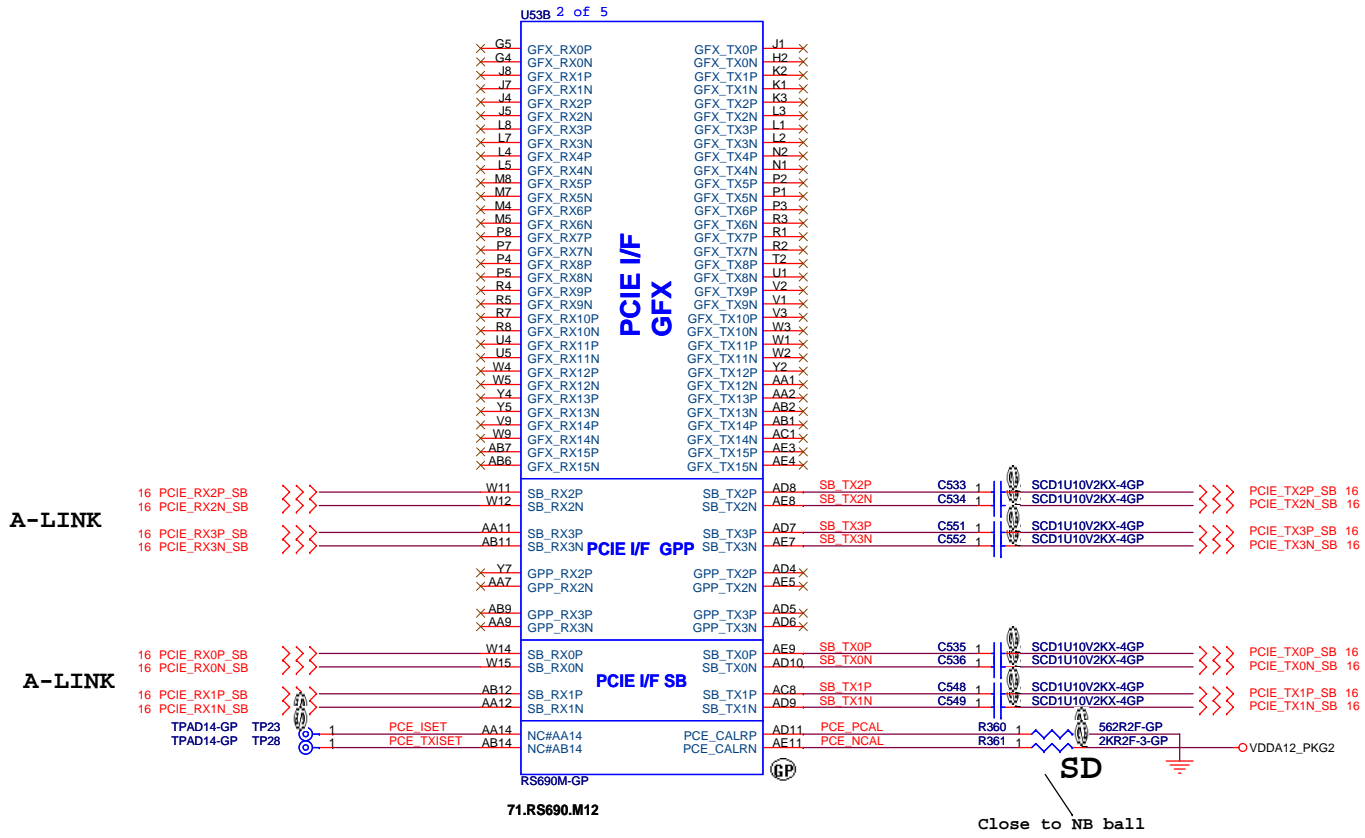


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**緯創資通 Wistron Corporation**  
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Title: **NB-RS690M HT**

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A-LINK

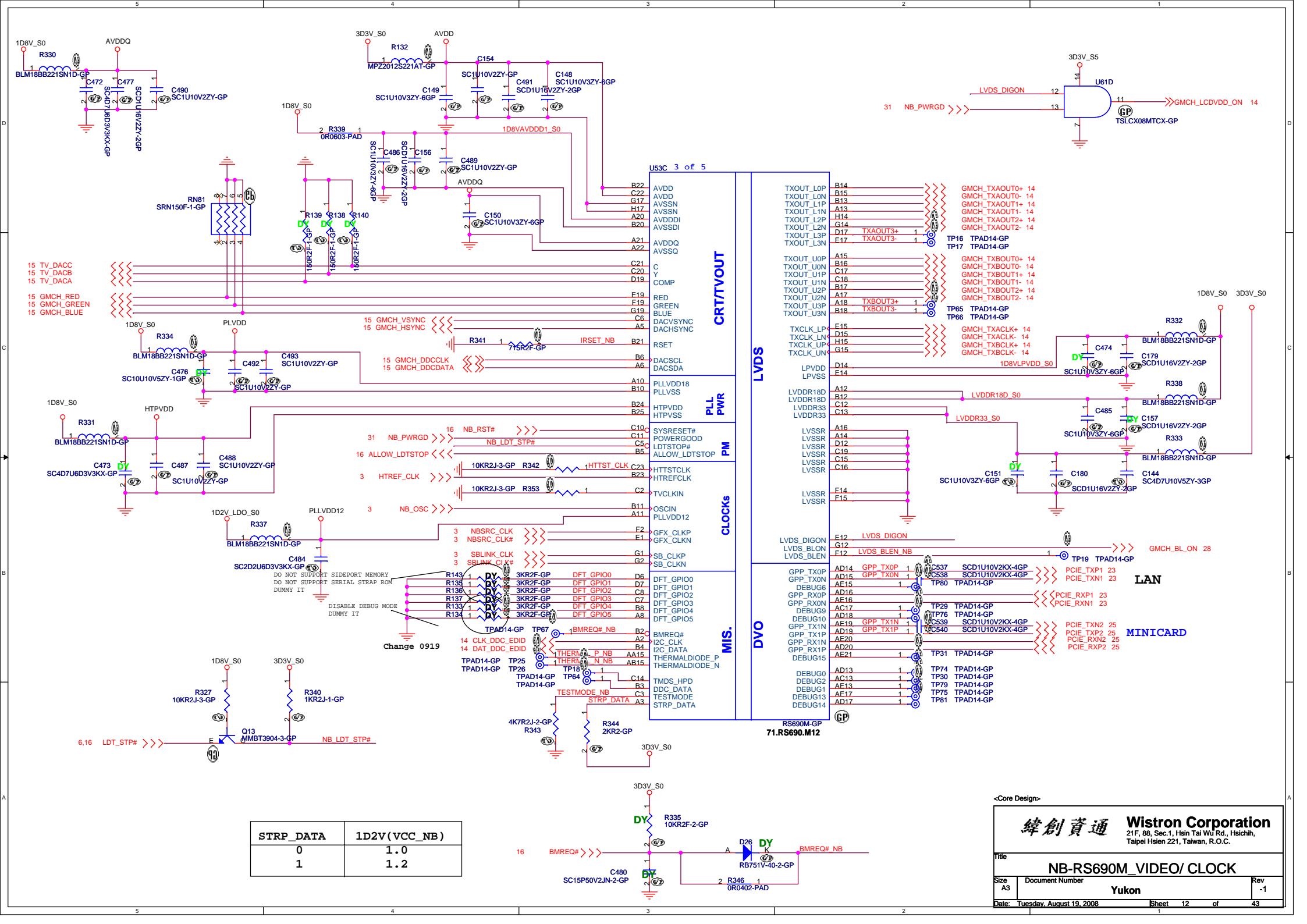
A-LINK

A-LINK

CLOSE TO NB

<Core Design>

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Title	
NB-RS690M_MEM/PCIE_LINK I/F	
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15 TV\_DACC  
15 TV\_DACB  
15 TV\_DACA

15 GMCH\_RED  
15 GMCH\_GREEN  
15 GMCH\_BLUE

15 GMCH\_VSYNC  
15 GMCH\_HSYNC

15 GMCH\_DDCCLK  
15 GMCH\_DDCDATA

31 NB\_PWRGD >>> NB\_RST# >>>  
16 ALLOW\_LDTSTOP <<< NB\_LDT\_STP# <<<  
3 HTREF\_CLK >>> 10KR2J-3-GP R342 1HTTST\_CLK B23  
3 NB\_OSC >>> 10KR2J-3-GP R353 1

3 NBSRC\_CLK >>> DFT GPIO0 D6  
3 NBSRC\_CLK# >>> DFT GPIO1 D7  
3 SBLINK\_CLK >>> DFT GPIO2 C8  
3 SBLINK\_CLK# >>> DFT GPIO3 C9  
3 SBLINK\_CLK# >>> DFT GPIO4 B8  
3 SBLINK\_CLK# >>> DFT GPIO5 A8

14 CLK\_DDC\_EDID >>> BMREQ# NB B2C  
14 DAT\_DDC\_EDID >>> I2C\_CLK A2  
TPAD14-GP TP25 THERM\_P\_NB AA15  
TPAD14-GP TP26 THERM\_N\_NB AB15

6.16 LDT\_STP# >>> Q13 MMBT3904-3-GP NB\_LDT\_STP#

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

16 BMREQ# >>> R346 1 0R0402-PAD

U53C 3 of 5

**CRTC/VOUT**

**LVDS**

**PLL PWR**

**PM**

**CLOCKS**

**MIS.**

**DVO**

RS690M-GP  
71.RS690.M12

B22 AVDD  
C22 AVDD  
G17 AVSSN  
H17 AVSSN  
A20 AVDDI  
B20 AVSSDI  
A21 AVDDQ  
A22 AVSSQ  
C21 C  
C20 Y  
D19 COMP  
F19 RED  
G19 GREEN  
C6 DACVSYNC  
A5 DACHSYNC  
B21 RSET  
B6 DACSCL  
A6 DACSDA  
A10 PLLVD18  
B10 PLLVSS  
B24 HTPVDD  
B25 HTPVSS  
C10C SYSRESET#  
C11 POWERGOOD  
C5 LDTSTOP#  
B5 ALLOW\_LDTSTOP  
C23 HTTSTCLK  
B23 HTREFCLK  
C2 TVCLKIN  
A11 OSCIN  
B11 PLLVD12  
E2 GFX\_CLKP  
E1 GFX\_CLKN  
G1 SB\_CLKP  
G2 SB\_CLKN

B14 GMCH\_TXAOUT0+ 14  
B15 GMCH\_TXAOUT0- 14  
B13 GMCH\_TXAOUT1+ 14  
A13 GMCH\_TXAOUT1- 14  
H14 GMCH\_TXAOUT2+ 14  
G14 GMCH\_TXAOUT2- 14  
D17 TXAOUT3+ 1  
E17 TXAOUT3- 1  
A15 GMCH\_TXBOUT0+ 14  
B16 GMCH\_TXBOUT0- 14  
C17 GMCH\_TXBOUT1+ 14  
C18 GMCH\_TXBOUT1- 14  
B17 GMCH\_TXBOUT2+ 14  
A17 GMCH\_TXBOUT2- 14  
A18 TXBOUT3+ 1  
B18 TXBOUT3- 1  
E15 GMCH\_TXACLK+ 14  
D15 GMCH\_TXACLK- 14  
G15 GMCH\_TXBCLK+ 14  
G15 GMCH\_TXBCLK- 14  
D14 LVDD18D  
E14 LVDDR18D  
B12 LVDDR18D  
C12 LVDDR18D  
C13 LVDDR33  
A12 LVDDR33  
B2 LVDDR33  
C13 LVDDR33

A16 LVSSR  
A14 LVSSR  
D12 LVSSR  
C19 LVSSR  
C15 LVSSR  
C16 LVSSR  
F14 LVSSR  
F15 LVSSR

E12 LVDS DIGON  
G12 LVDS\_BLEN NB  
F12 LVDS\_BLEN NB

AD14 GPP\_TX0P 1  
AD15 GPP\_TX0N 1  
AE15 GPP\_TX0N 1  
AD16 GPP\_RX0P 1  
AE16 GPP\_RX0N 1  
AC17 GPP\_TX1N 1  
AD18 GPP\_TX1P 1  
AE19 GPP\_TX1P 1  
AD20 GPP\_RX1N 1  
AE21 GPP\_RX1P 1  
AD13 GPP\_TX0P 1  
AC13 GPP\_TX0N 1  
AE13 GPP\_TX0N 1  
AD17 GPP\_RX1N 1  
AE17 GPP\_RX1P 1  
AD17 GPP\_RX1P 1

TP29 TPAD14-GP  
TP76 TPAD14-GP  
TP76 TPAD14-GP  
TP79 TPAD14-GP  
TP75 TPAD14-GP  
TP81 TPAD14-GP

TP16 TPAD14-GP  
TP17 TPAD14-GP  
TP65 TPAD14-GP  
TP66 TPAD14-GP  
TP19 TPAD14-GP

C537 SCD1U10V2KX-4GP  
C538 SCD1U10V2KX-4GP  
C539 SCD1U10V2KX-4GP  
C540 SCD1U10V2KX-4GP

PCIE\_TXP1 23  
PCIE\_TXN1 23  
PCIE\_RXP1 23  
PCIE\_RXN1 23  
PCIE\_TXN2 25  
PCIE\_RXN2 25  
PCIE\_RXP2 25

LAN

MINICARD

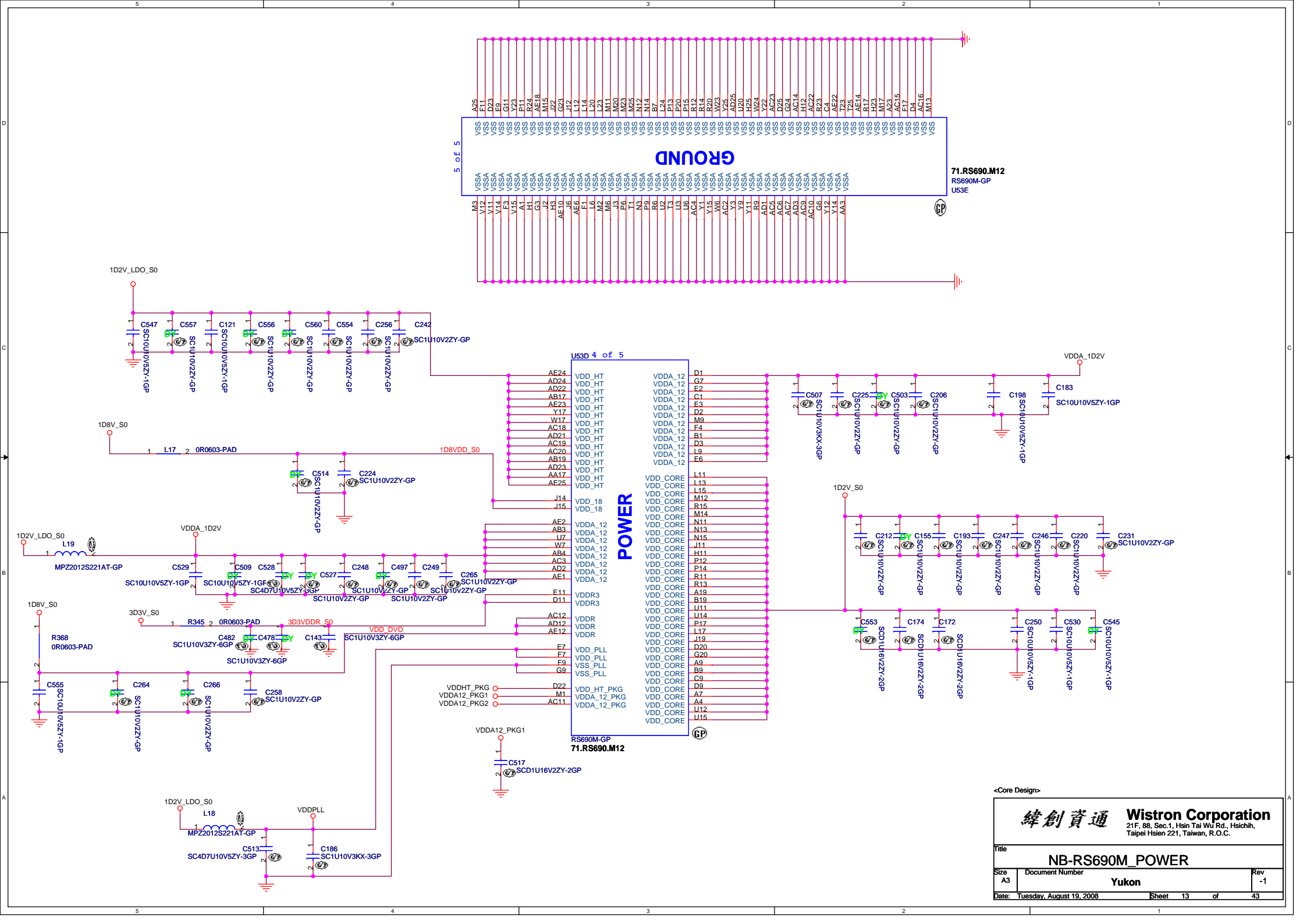
<Core Design>

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Title: **NB-RS690M\_VIDEO/ CLOCK**

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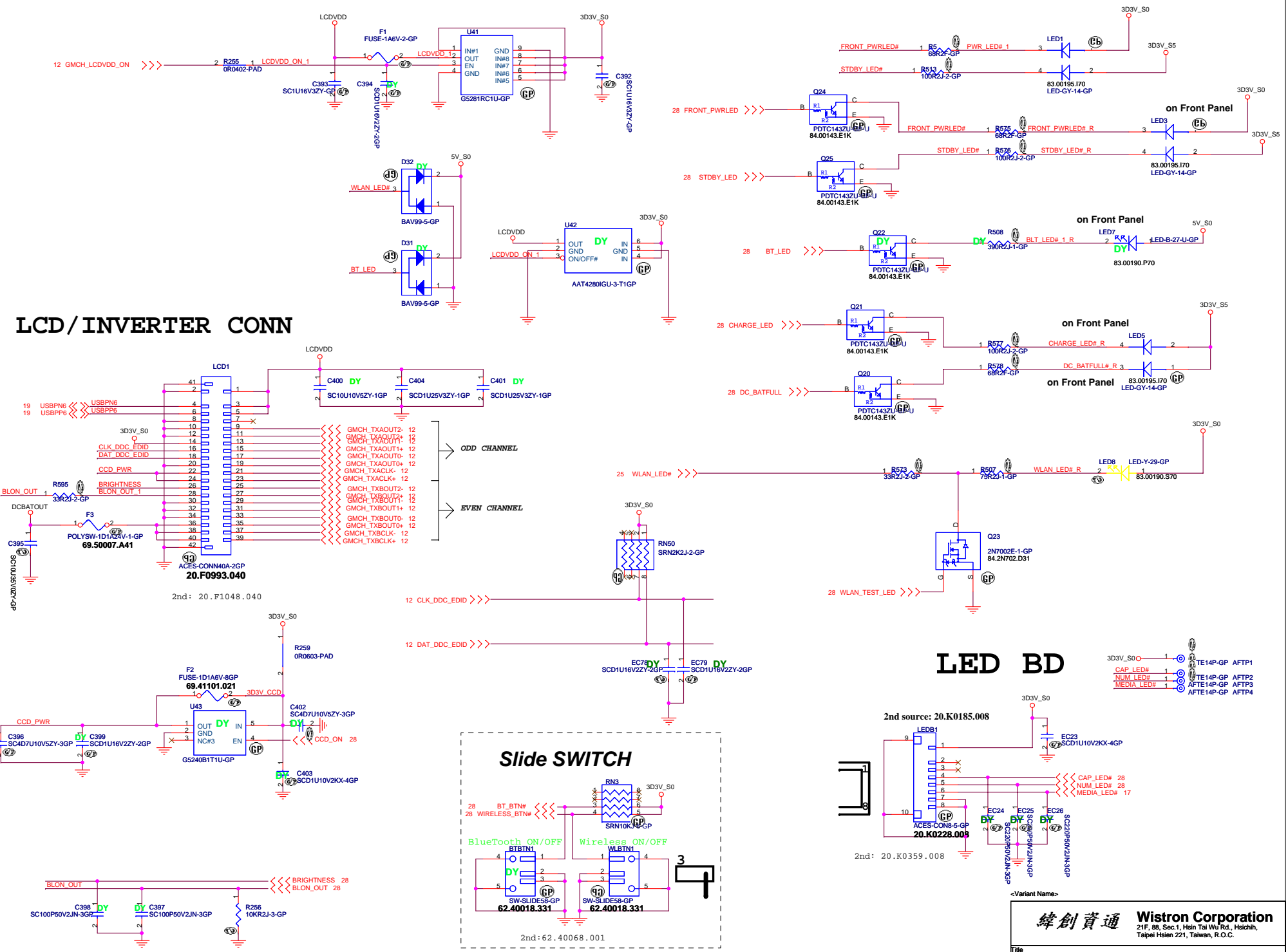
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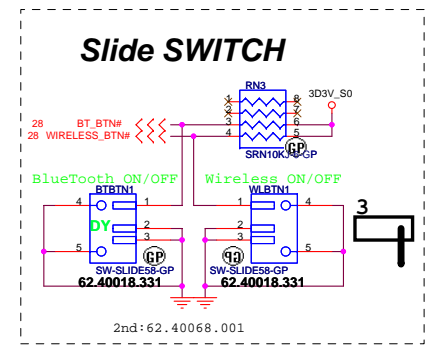
Title: **NB-RS690M\_POWER**

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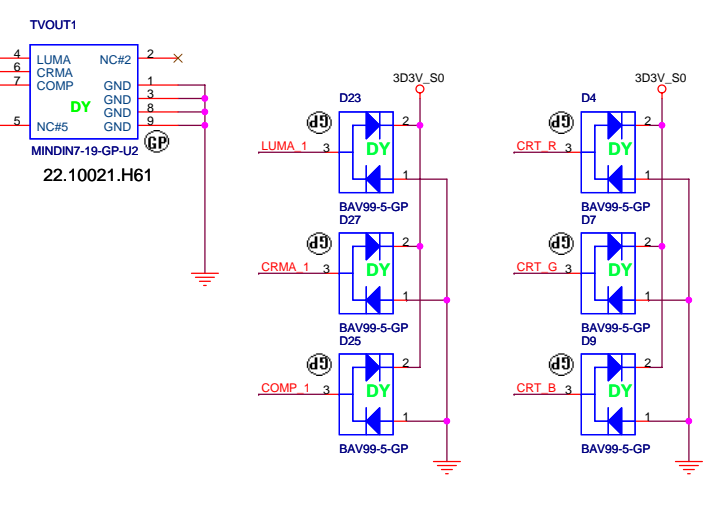
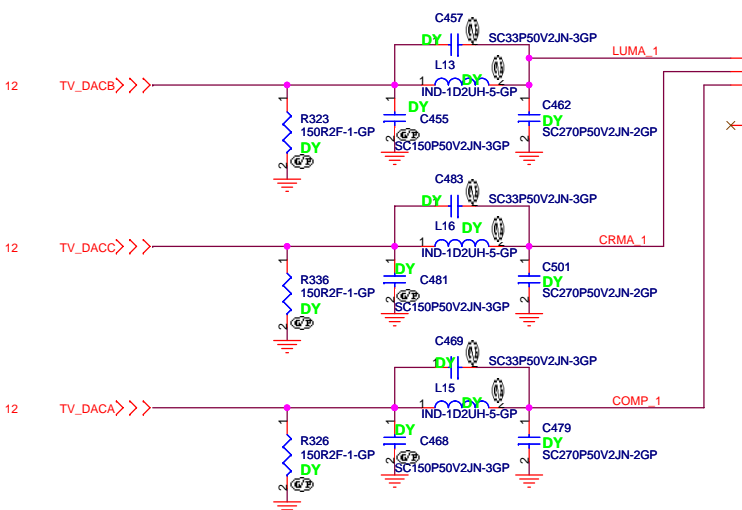
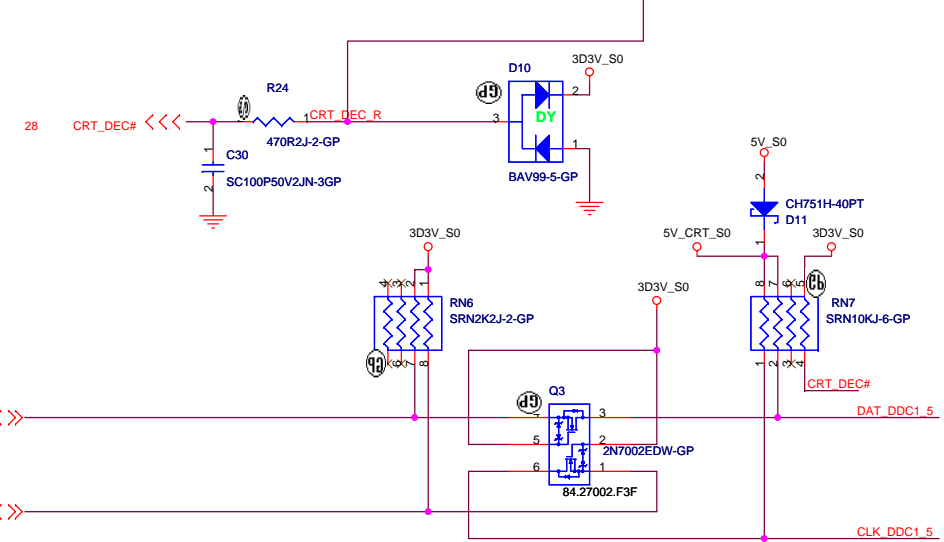
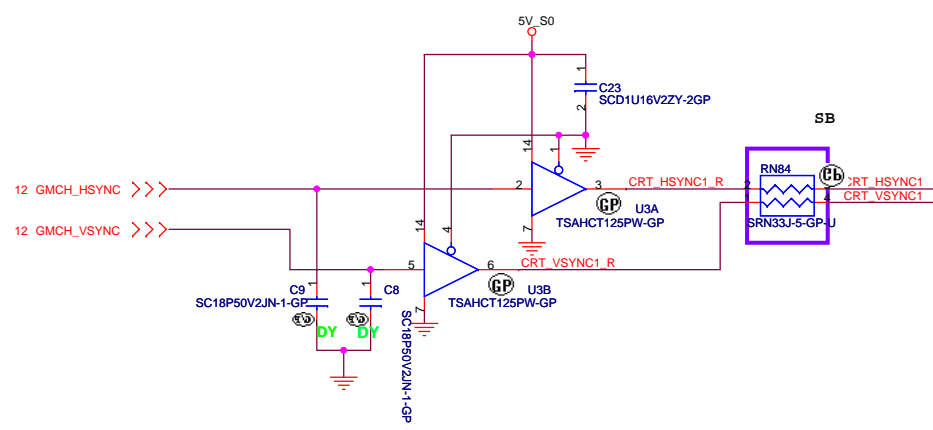
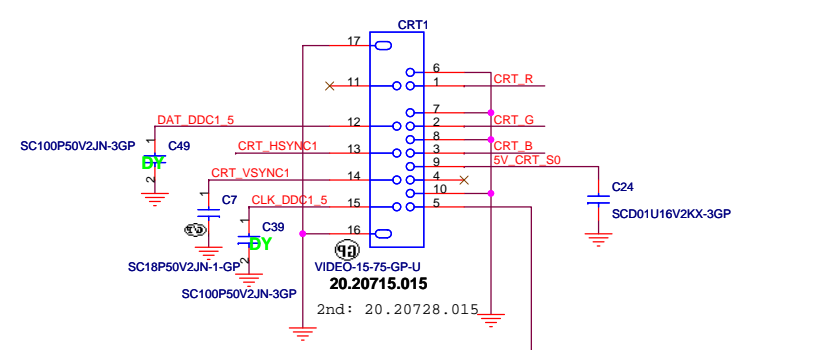
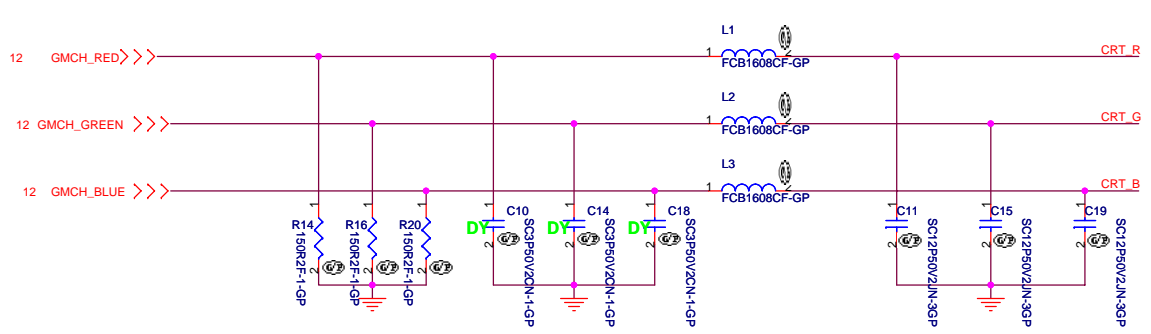
# LCD/INVERTER CONN



## LED BD



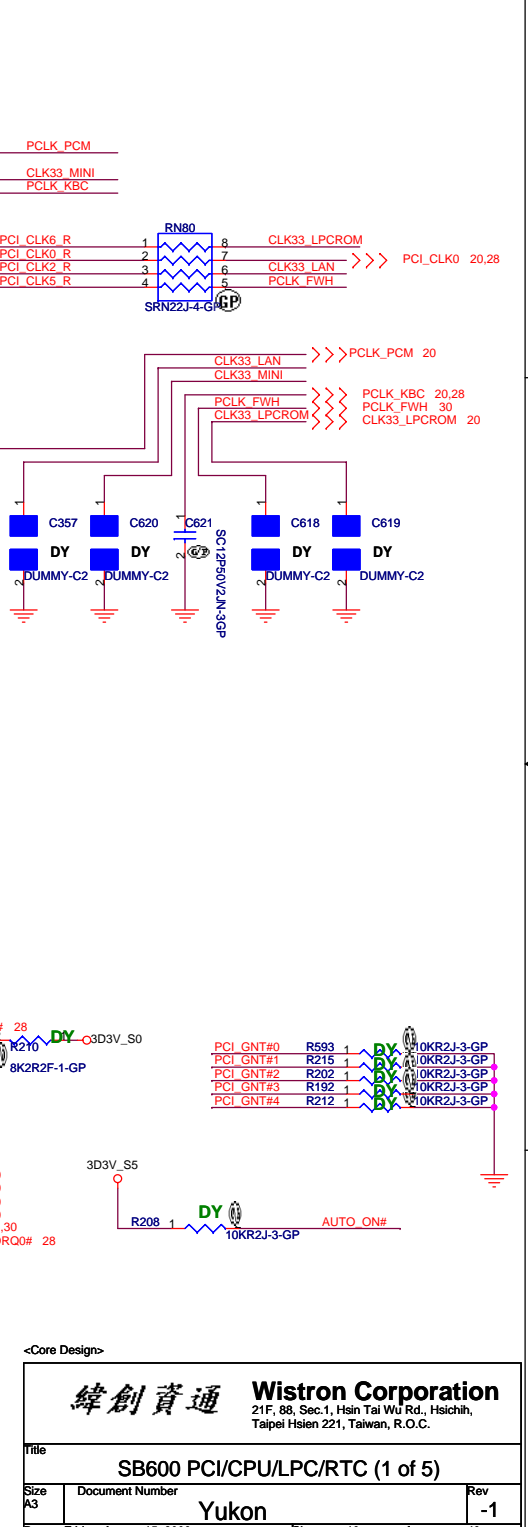
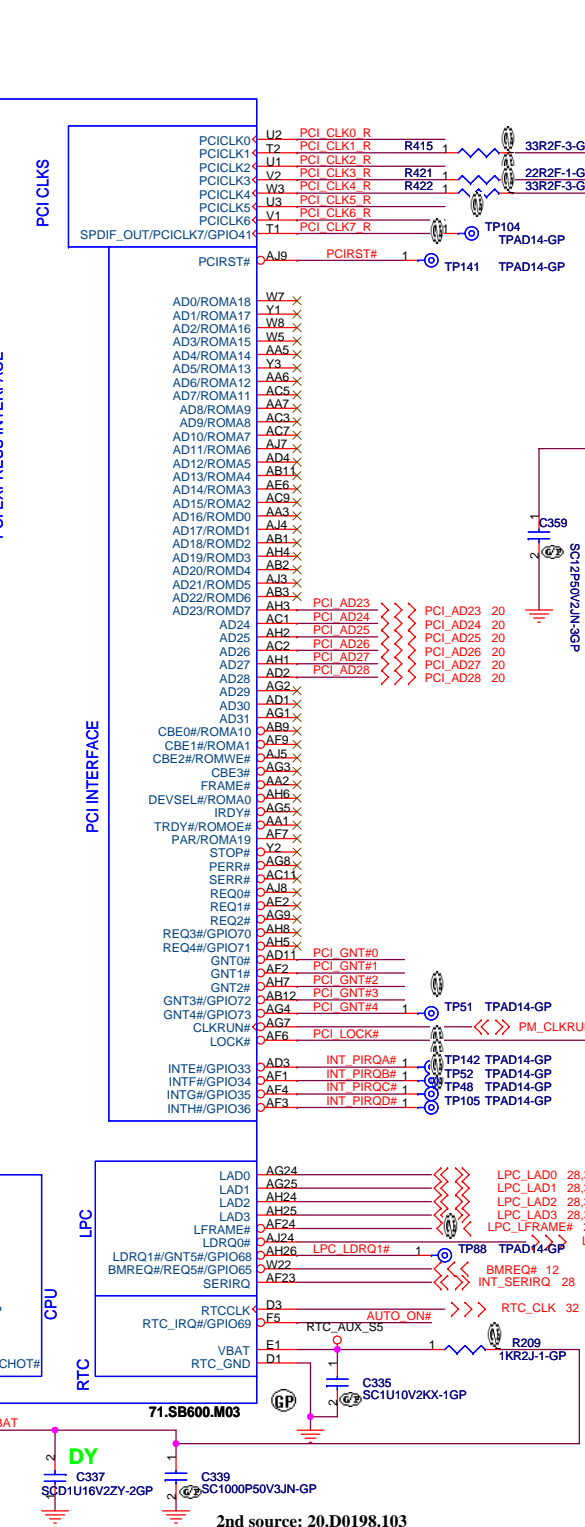
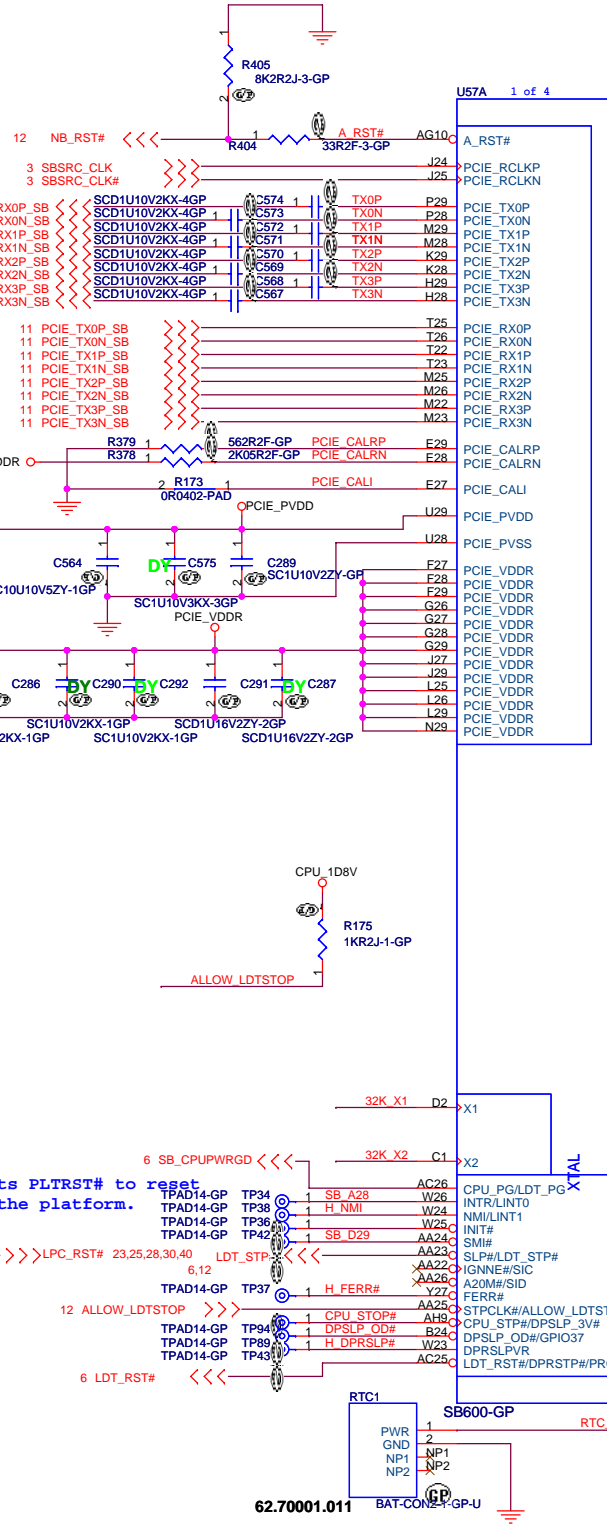
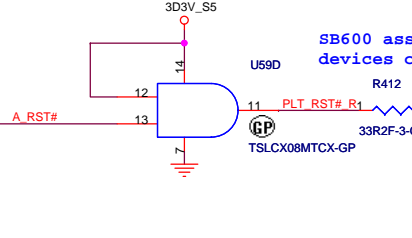
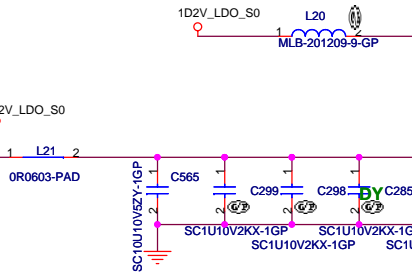
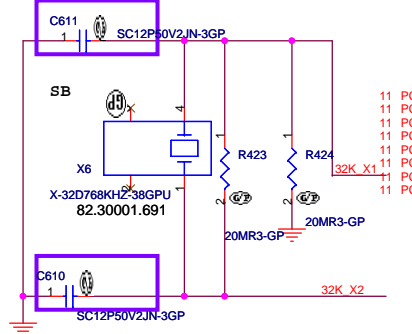
## Slide SWITCH



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Title		<b>CRT/TV Connector</b>	
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Place these components close to U13 and use ground guard for 32K\_X1 and 32K\_X2.



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Title: **SB600 PCI/CPU/LPC/RTC (1 of 5)**

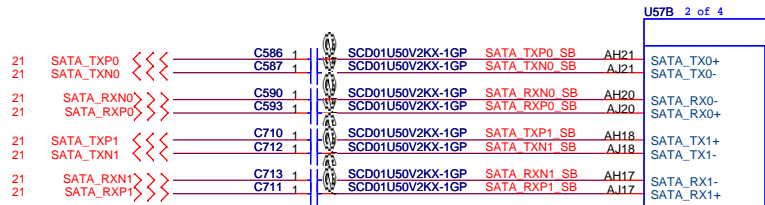
Size: A3 Document Number: Yukon Rev: -1

Date: Friday, August 15, 2008 Sheet: 16 of 43

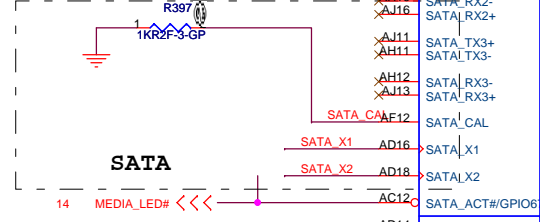
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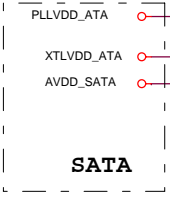
PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460



SATA

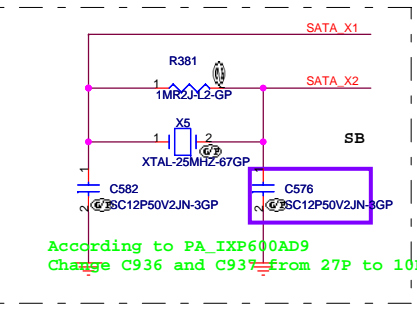


SATA

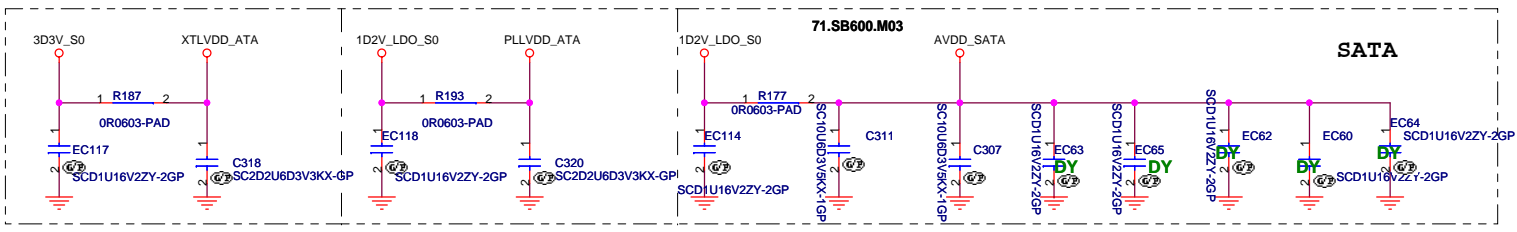
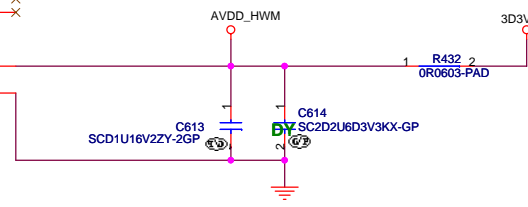
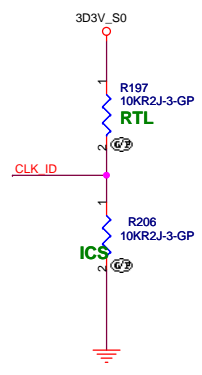
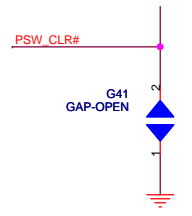
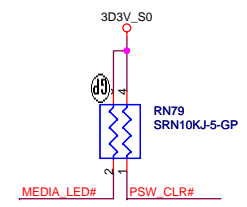
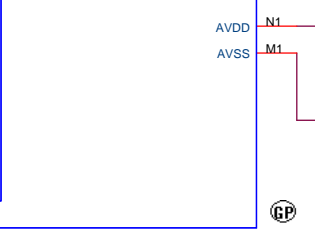
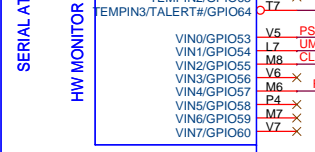
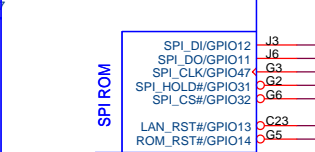
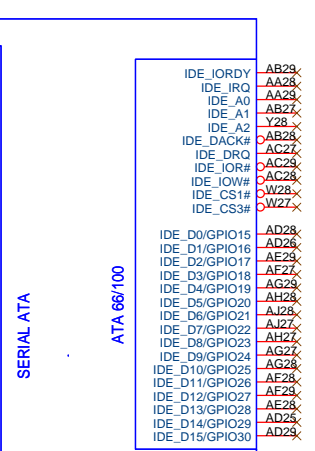


SATA

SATA



According to PA\_IXP600AD9  
Change C936 and C937 from 27P to 10P.



<Core Design>

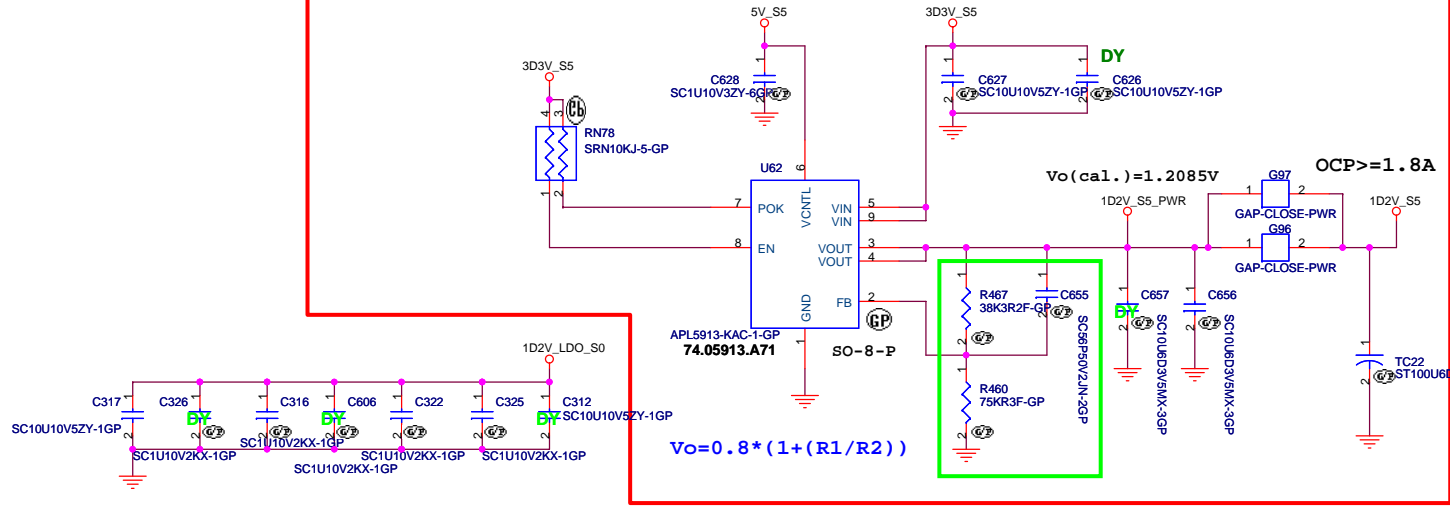
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 ACPI/GPIO/SATA/IDE (2 of 5)**

A3 Document Number: **Yukon** Rev: **-1**

Date: Friday, August 15, 2008 Sheet 17 of 43

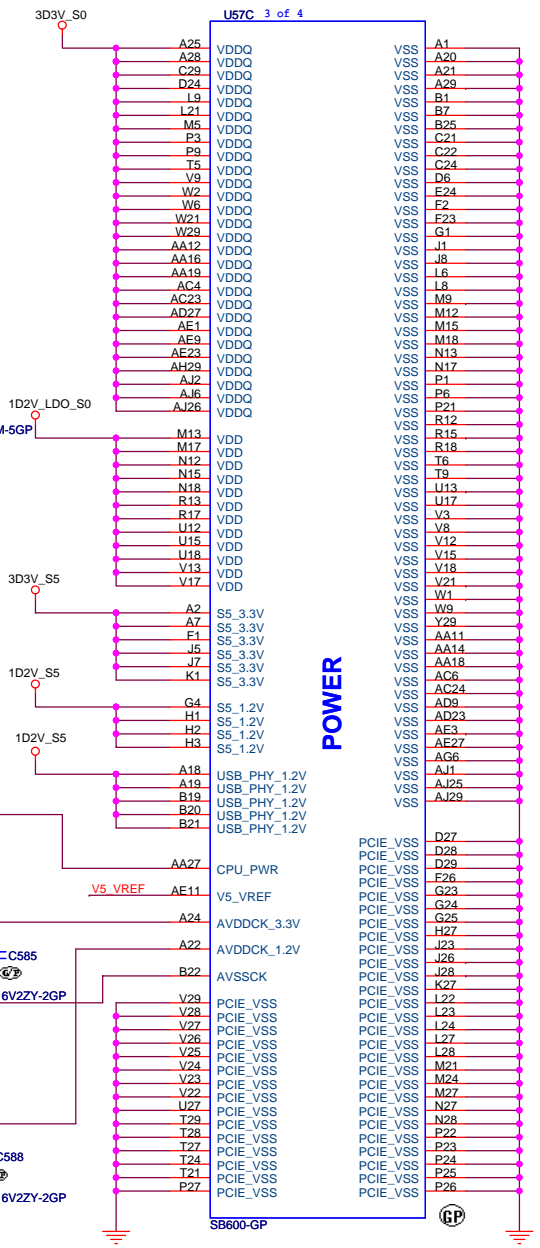
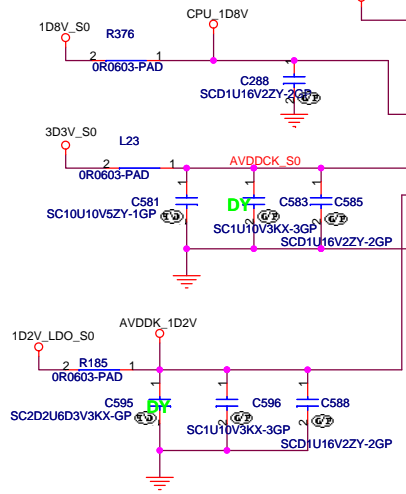
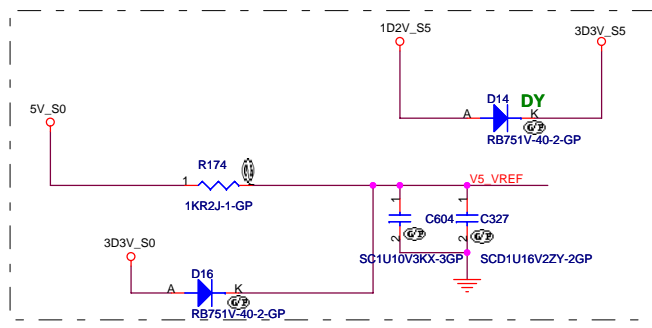
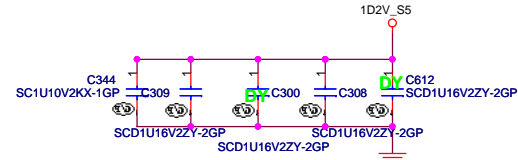
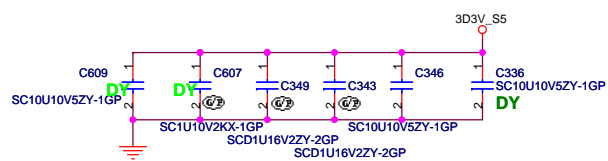
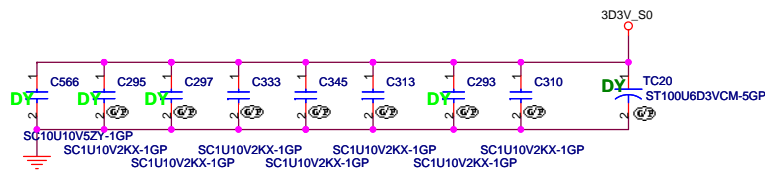
1D2V\_S5  
Iomax=1A



$$V_o = 0.8 * (1 + (R1/R2))$$

$V_o(\text{cal.}) = 1.2085V$   
OCP >= 1.8A

Place near to SB600



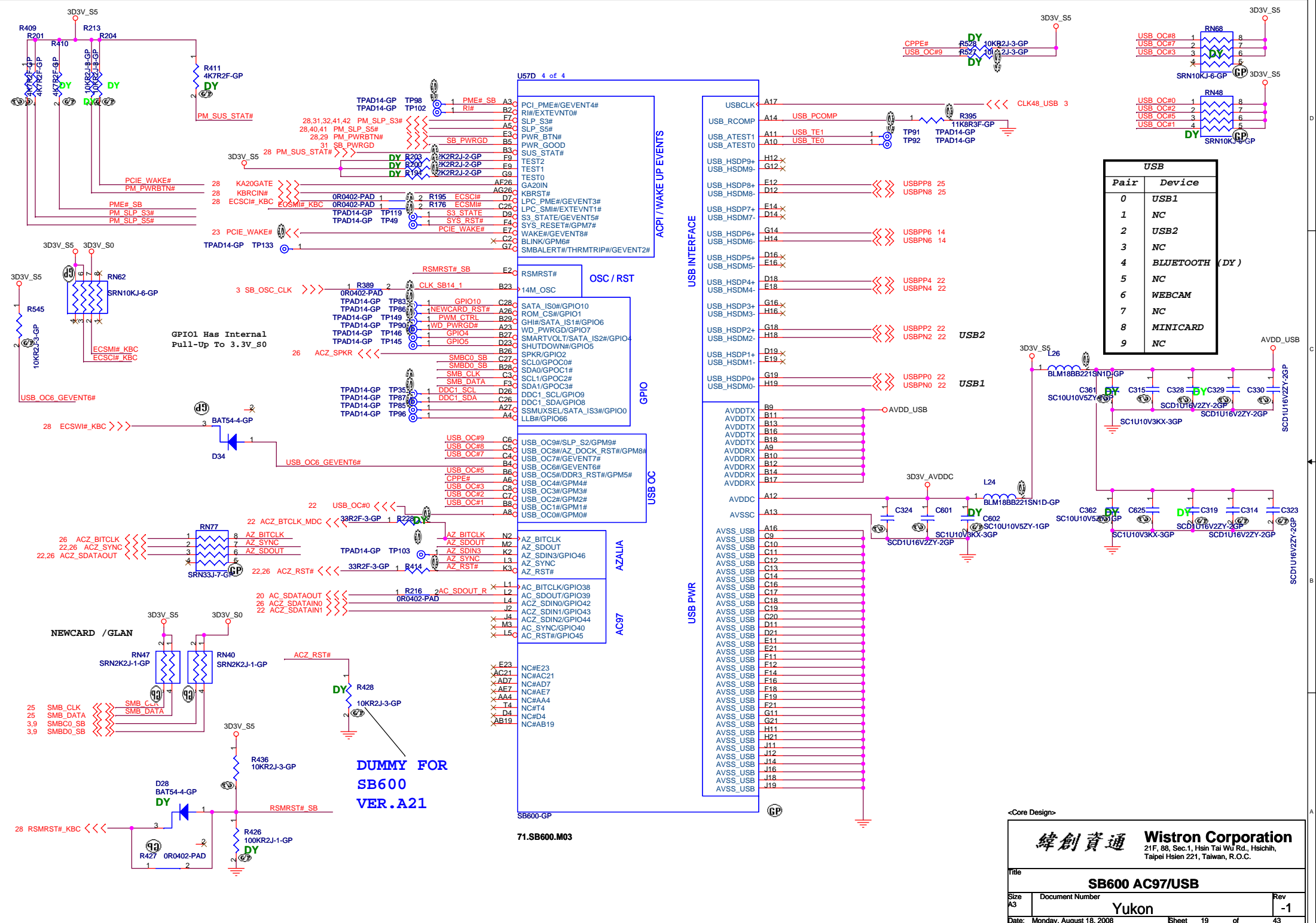
71.SB600.M03

<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 POWER/DECOUPLING**

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Date: Wednesday, August 13, 2008	Sheet 18 of 43	



USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	BLUETOOTH (DY)
5	NC
6	WEBCAM
7	NC
8	MINICARD
9	NC

DUMMY FOR SB600 VER. A21

71.SB600.M03

<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

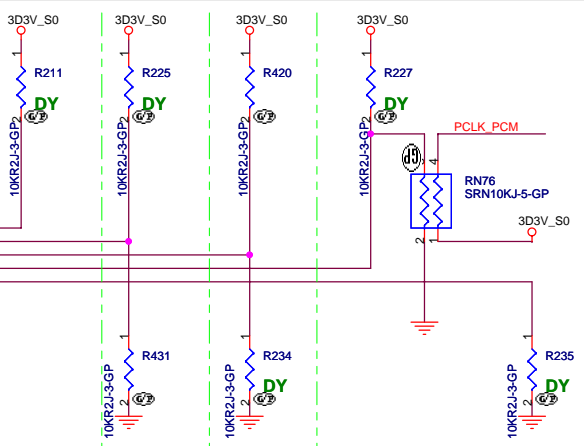
Title: **SB600 AC97/USB**

Size A3 Document Number: **Yukon** Rev: **-1**

Date: Monday, August 18, 2008 Sheet 19 of 43

PCI\_CLK4  
PCI\_CLK6  
PCI\_CLK0  
PCI\_CLK1

19 AC\_SDATAOUT  
16,28 PCLK\_KBC  
15 CLK33\_LPCROM  
16,28 PCI\_CLK0  
16 PCLK\_PCM

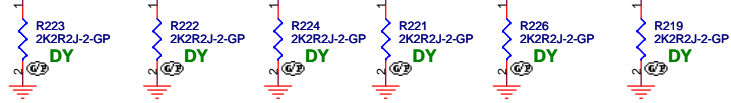


**REQUIRED SYSTEM STRAPS**

		SB600				
		AC_SDATAOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM		
	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	L, H = LPC ROM L, L = FWH ROM DEFAULT		

**SB600 HAS 15K INTERNAL PU FOR PCI\_AD[23..28]**

16 PCI\_AD28  
16 PCI\_AD27  
16 PCI\_AD26  
16 PCI\_AD25  
16 PCI\_AD24  
16 PCI\_AD23



**DEBUG STRAPS**

	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW				USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

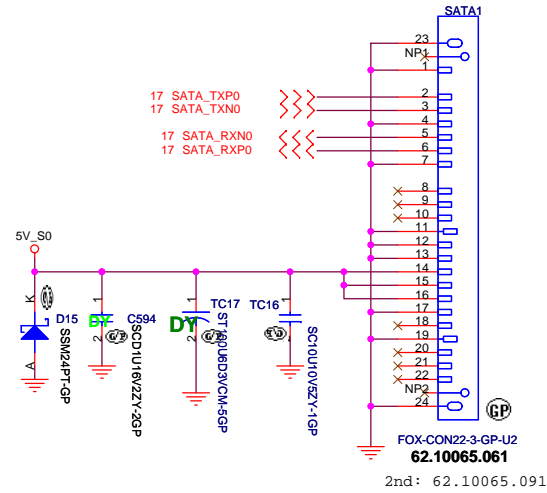
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB600 STRAPPING PIN**

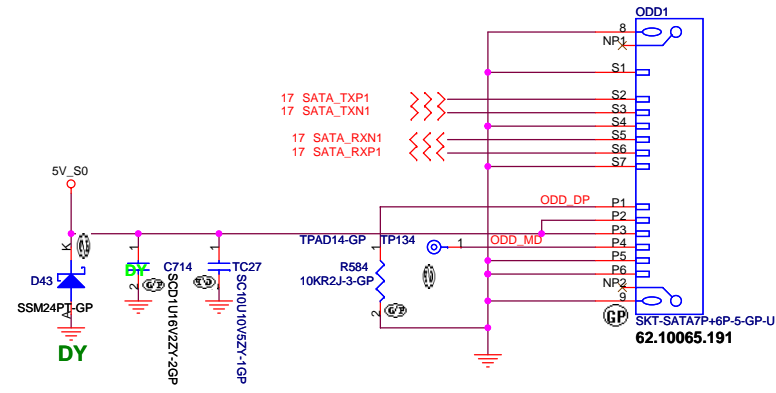
Size A3 Document Number Yukon Rev -1

Date: Monday, August 18, 2008 Sheet 20 of 43

# SATA HD Connector

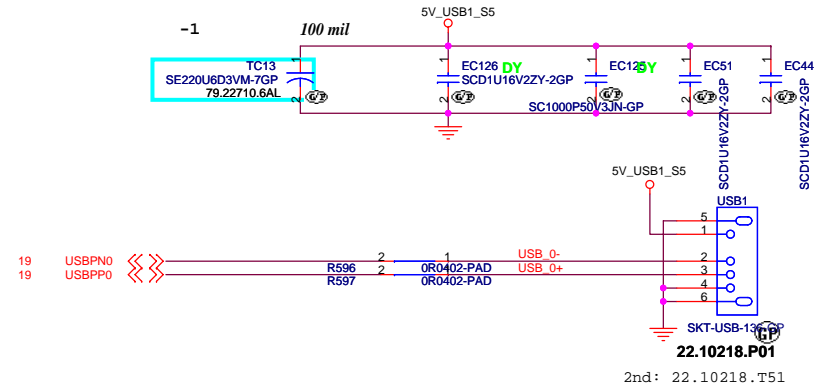
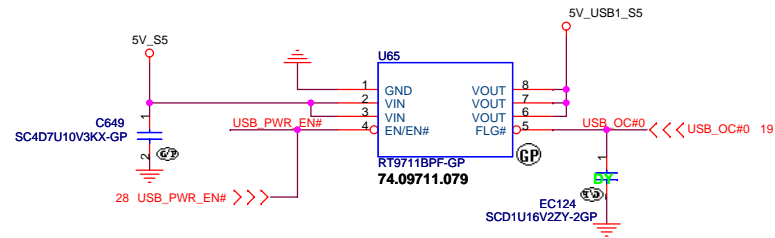


# SATA ODD Connector



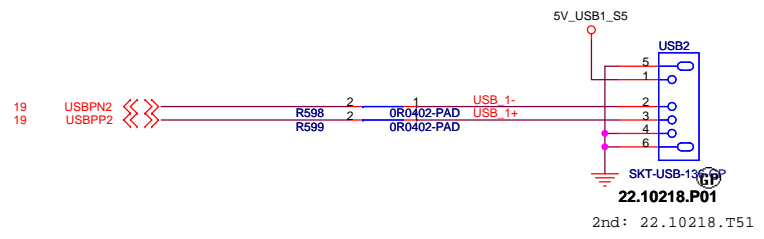
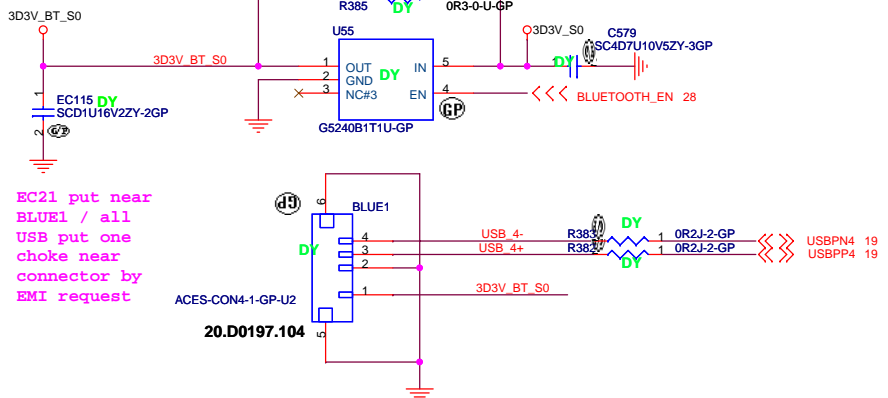
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<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>HDD and CDROM</b>	
<b>Size</b> Document Number	<b>Rev</b> -1
<b>Yukon</b>	
<b>Date:</b> Thursday, August 14, 2008	<b>Sheet</b> 21 <b>of</b> 43



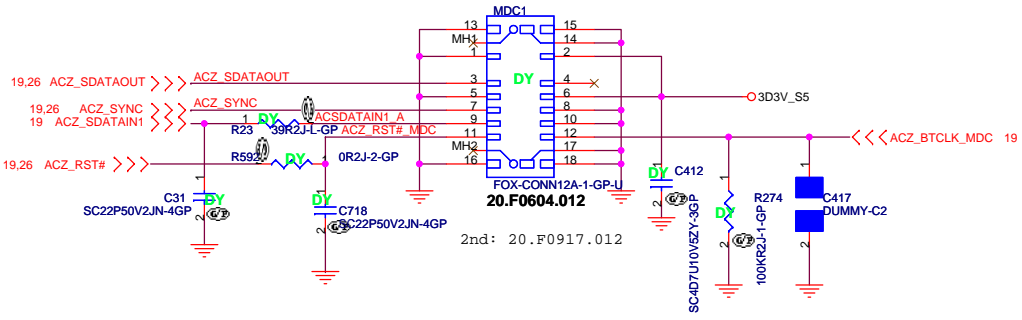
2nd: 22.10218.T51

### BLUETOOTH MODULE

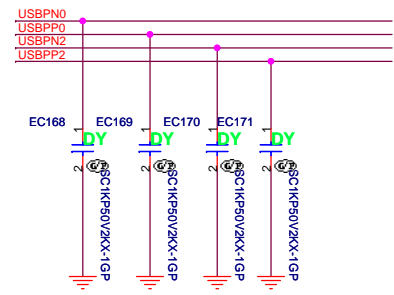


2nd: 22.10218.T51

### MDC 1.5 CONN

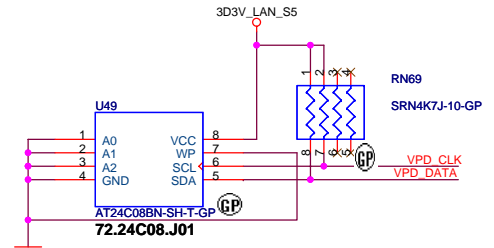
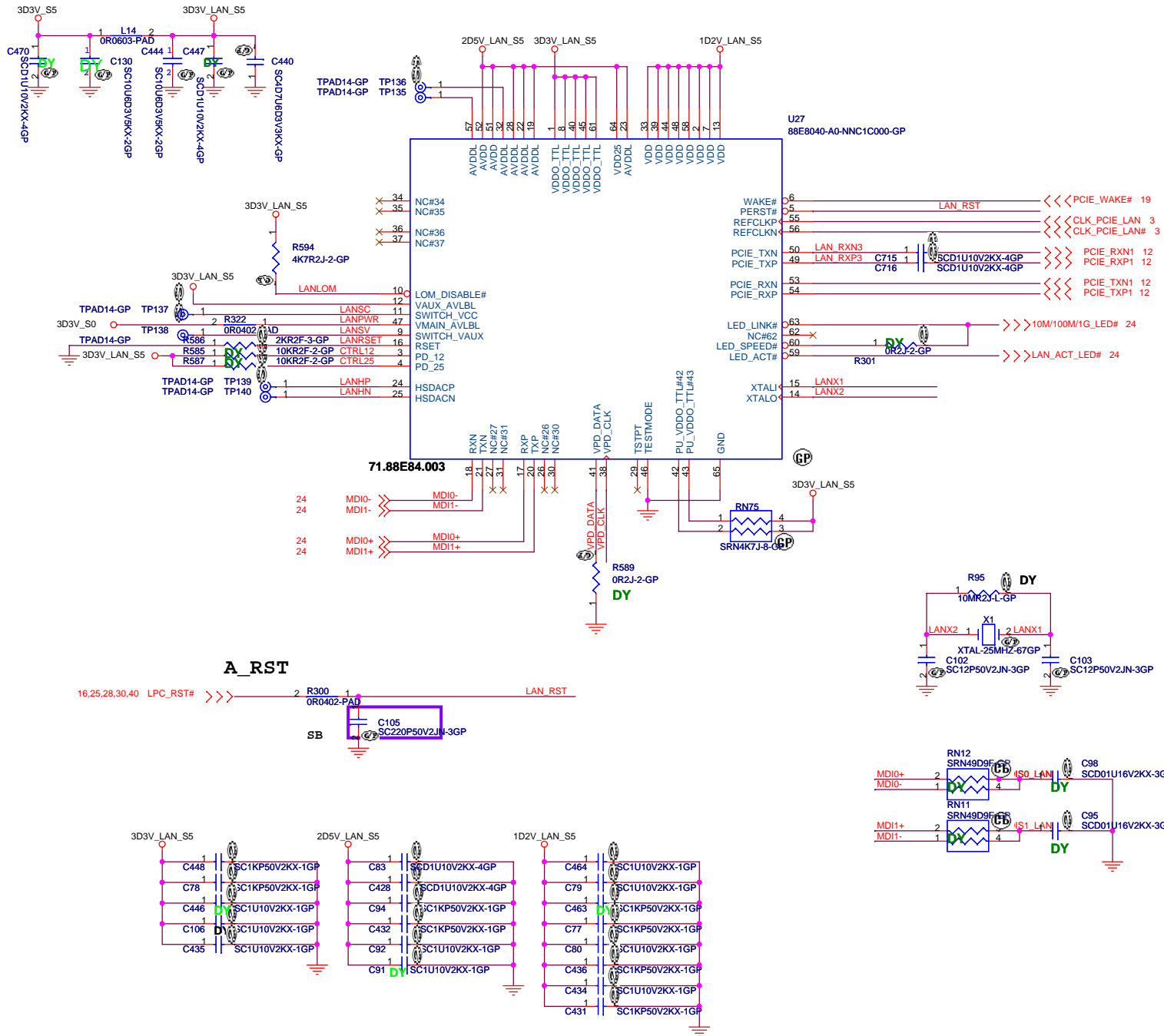


2nd: 20.F0917.012



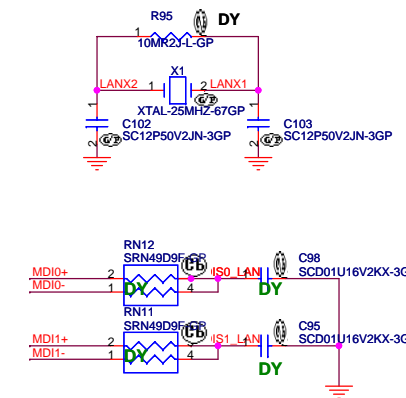
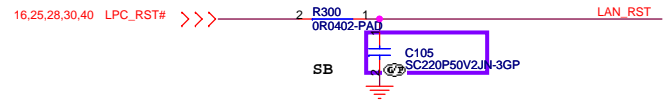
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB / MDC / BLUETOOTH</b>			
Title	Document Number		Rev
	<b>Yukon</b>		-1
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Pull up for AT24C08 another pull low

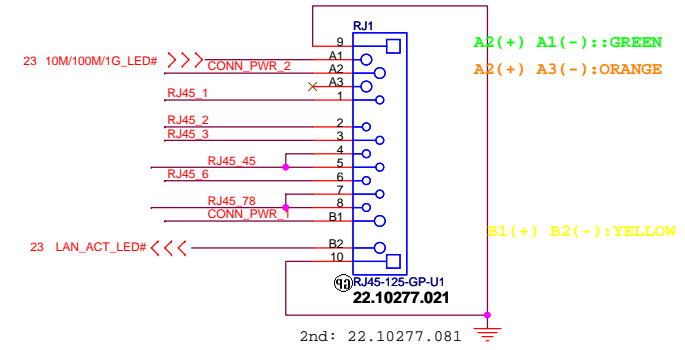
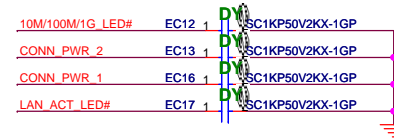
**A\_RST**



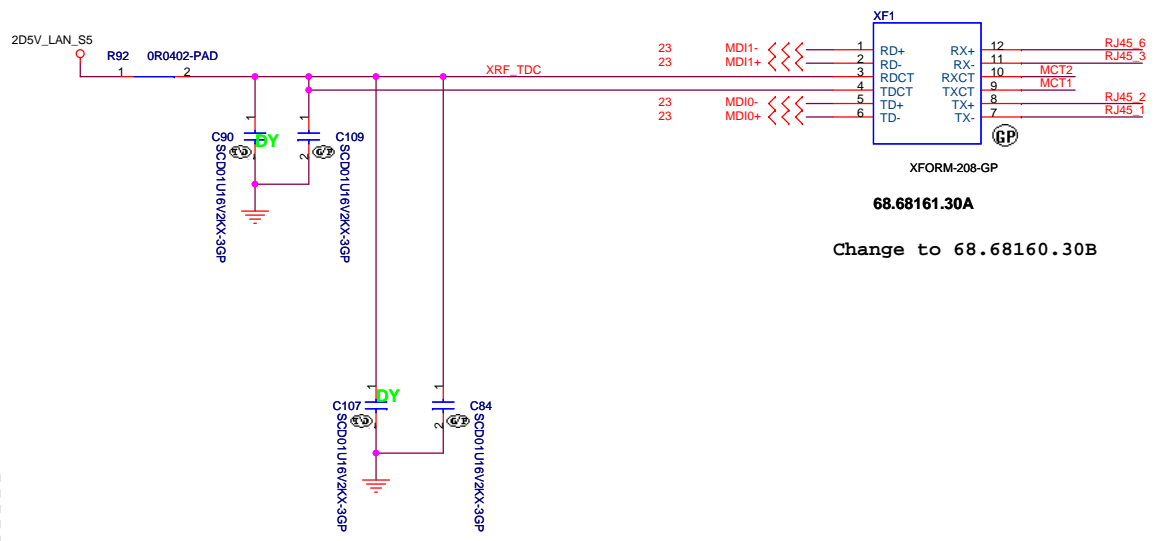
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>MARVELL 88E8040</b>			
Size	Document Number	Rev	
A3	Yukon	-1	
Date:	Thursday, August 14, 2008	Sheet	23 of 43

# LAN Connector



## 10/100 Lan Transformer



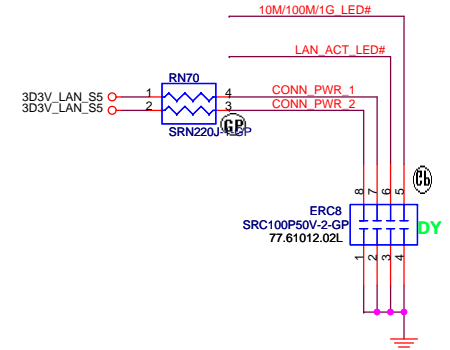
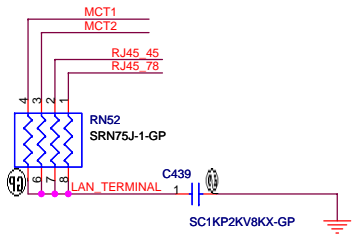
Change to 68.68160.30B

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Variant Name>

**緯創資通 Wistron Corporation**  
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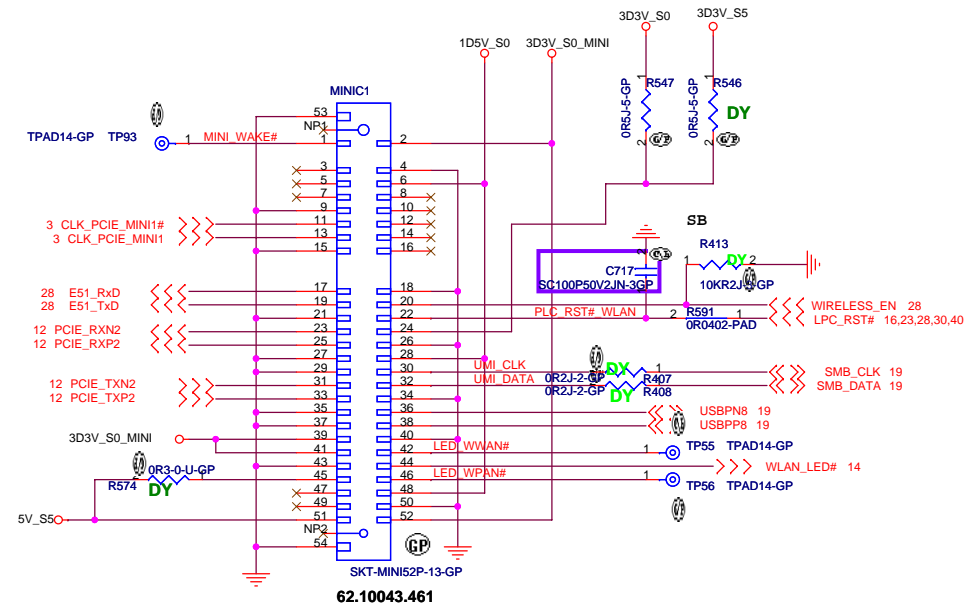
Title: **LAN Connector**

Size A3 Document Number **Yukon** Rev **-1**

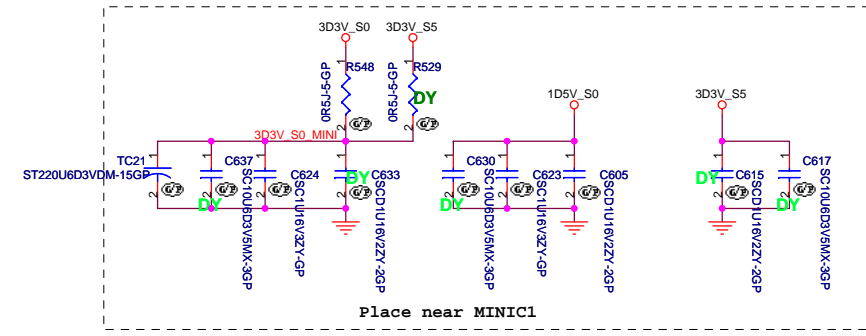
Date: Wednesday, August 13, 2008 Sheet 24 of 43



# Mini Card Connector



2nd: 20.F1049.052



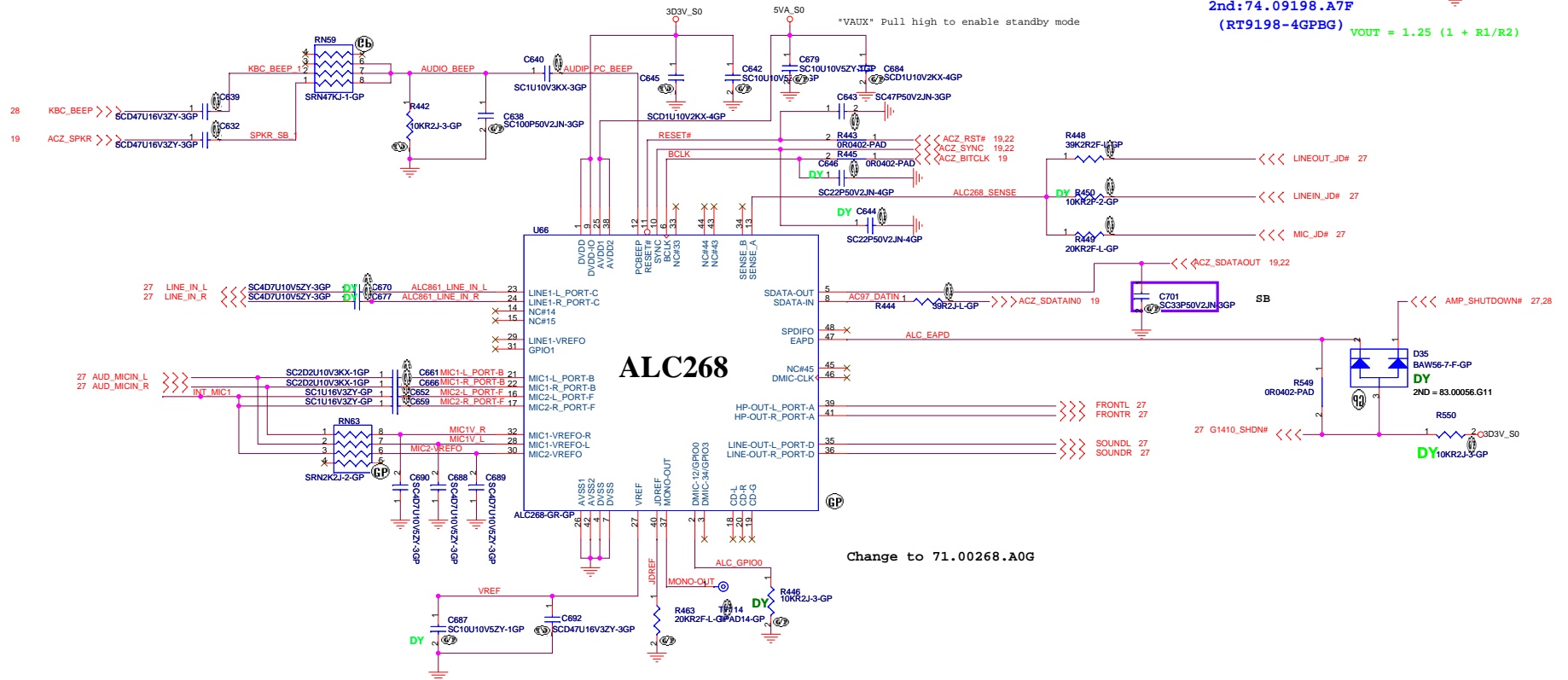
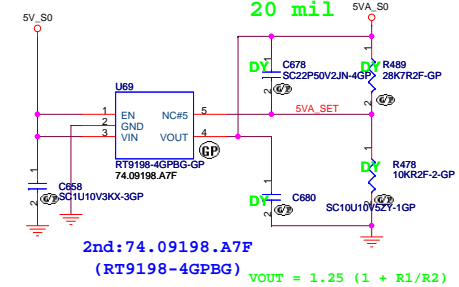
bom1

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>MINI CARD</b>			
Size	Document Number		Rev
	<b>Yukon</b>		-1
Date:	Thursday, August 14, 2008		Sheet 25 of 43

# POWER GENERATE

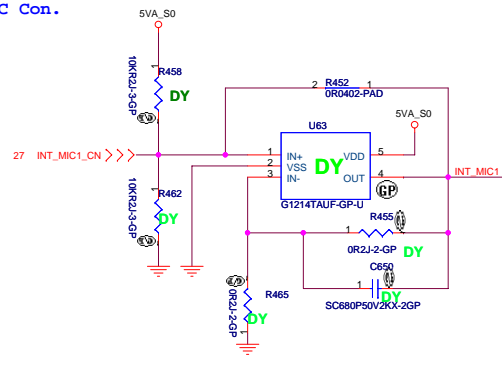
\*Layout\*

20 mil



Change to 71.00268.A0G

Near INTMIC Con.



<-Variant Name>

緯創資通 Wistron Corporation  
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

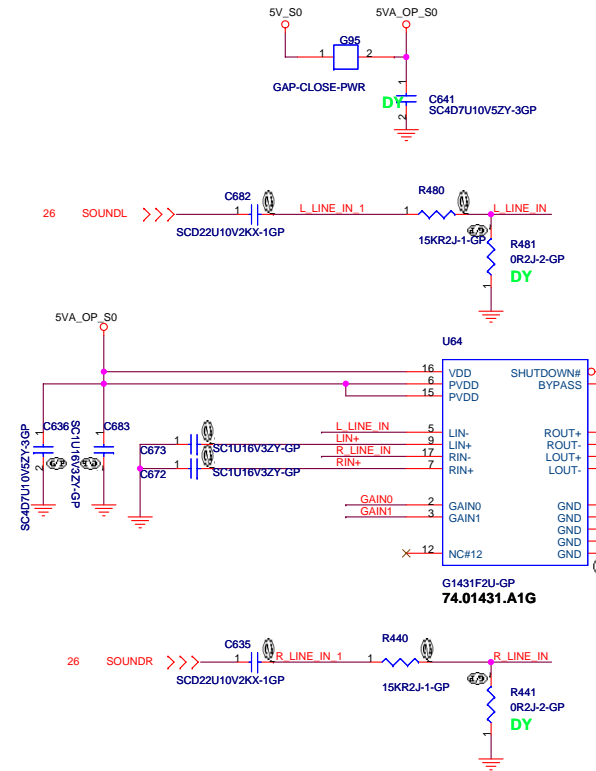
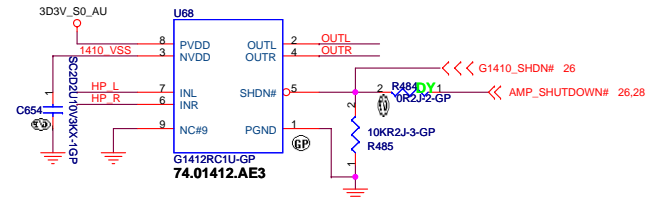
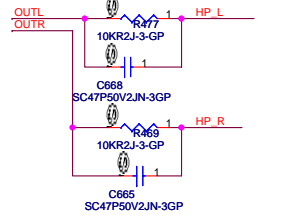
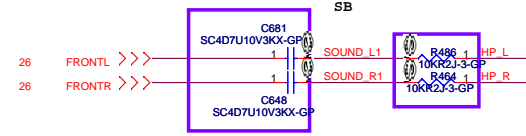
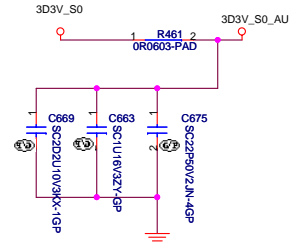
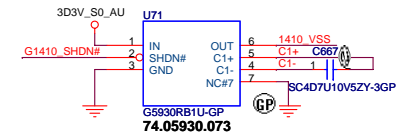
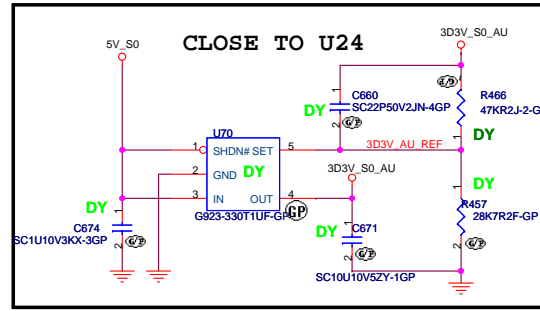
Title AZALIA CODEC - ALC268

Size Document Number Yukon Rev -1

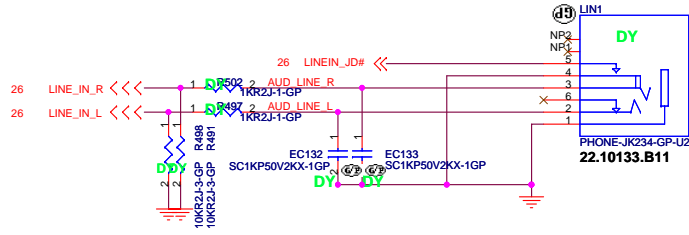
Date: Thursday, August 14, 2008 Sheet 26 of 43

# AUDIO OP AMPLIFIER

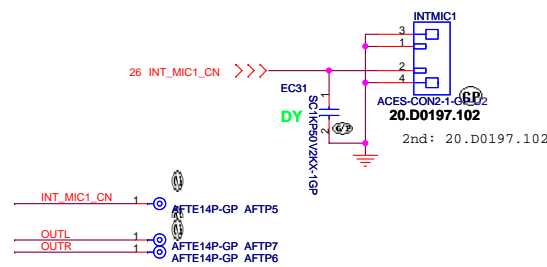
KBC\_MUTE\_GPIO8



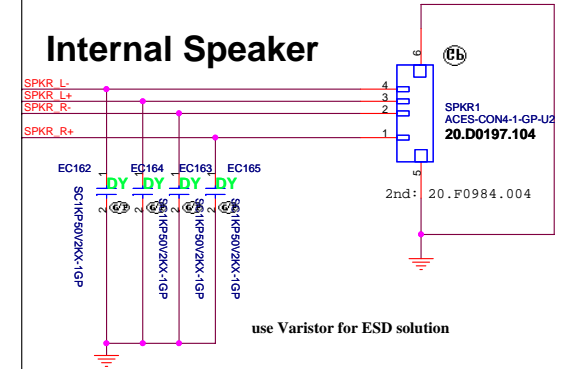
## LINE IN



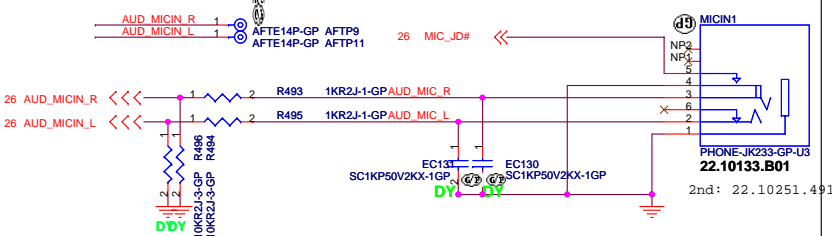
## Internal Microphone



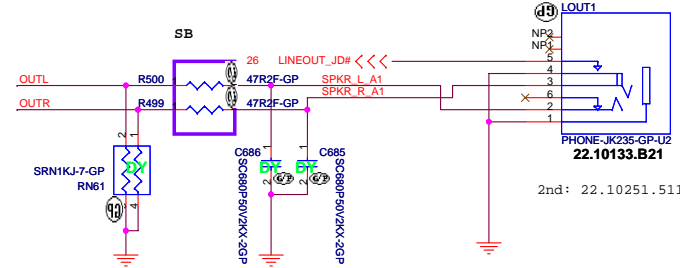
## Internal Speaker

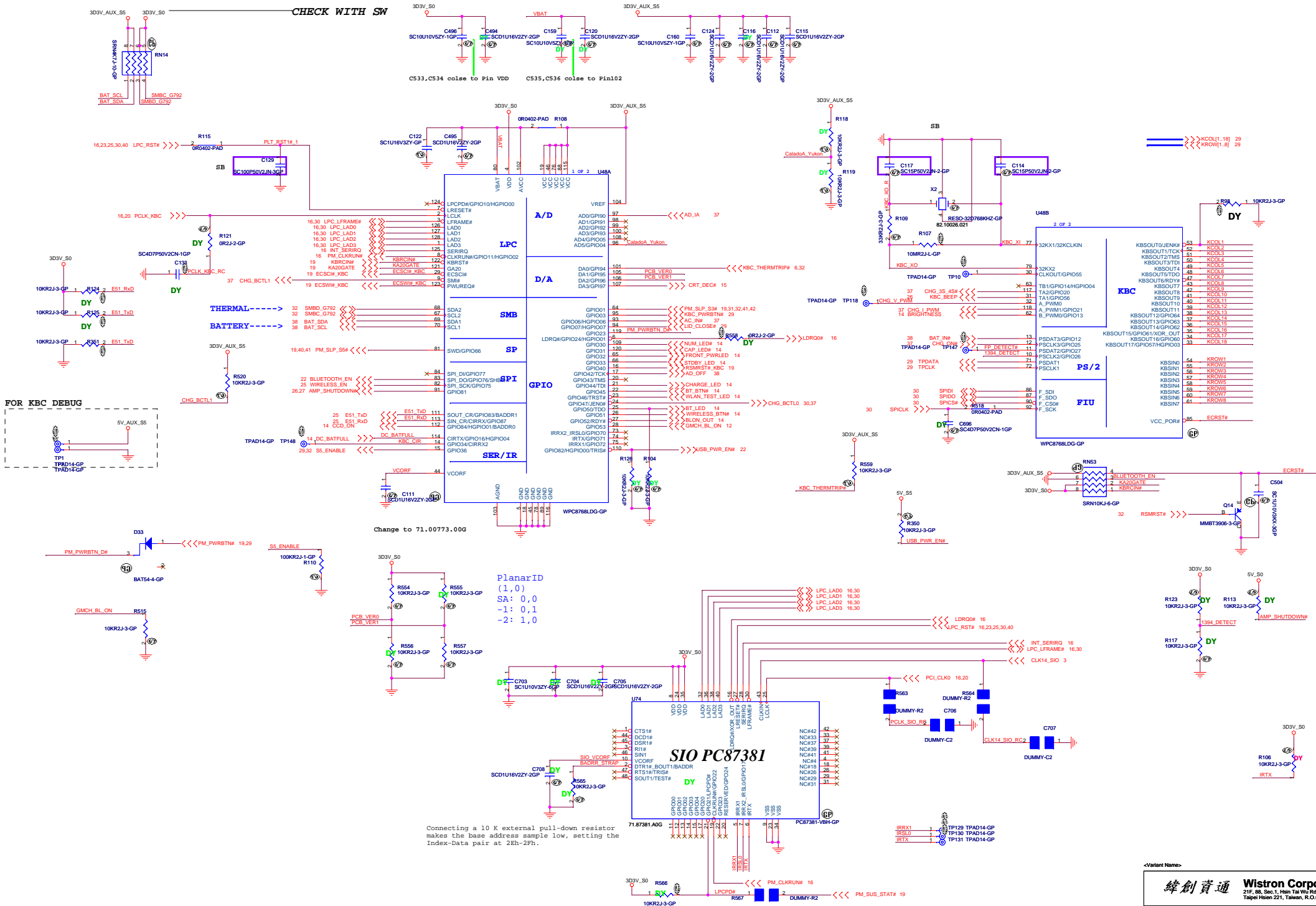


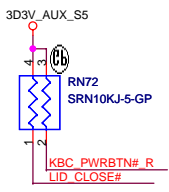
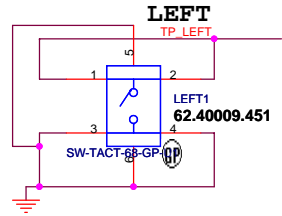
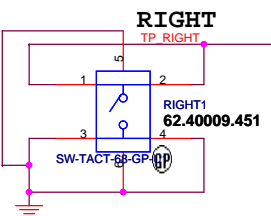
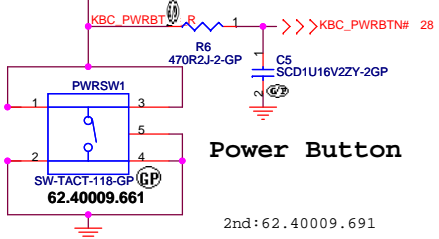
## MIC IN



## LINE OUT

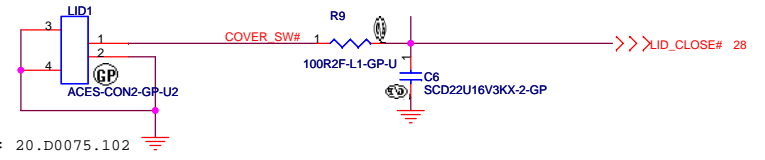




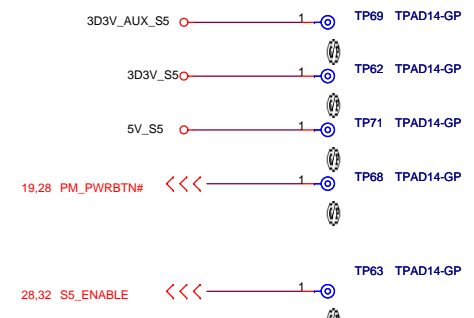


### Cover Up Switch

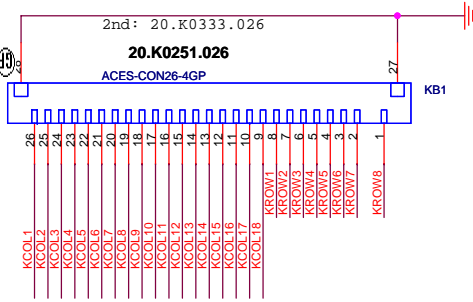
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### Check test point



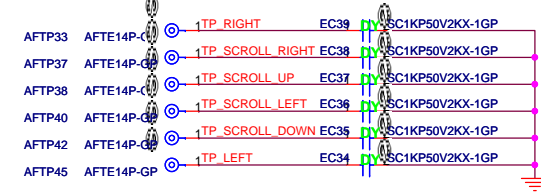
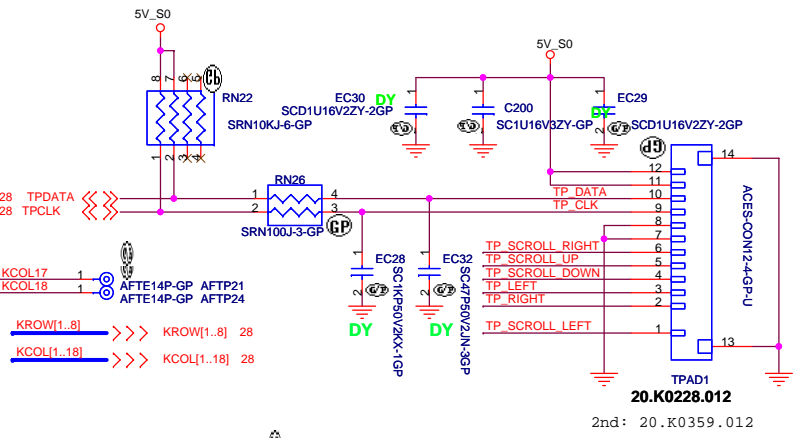
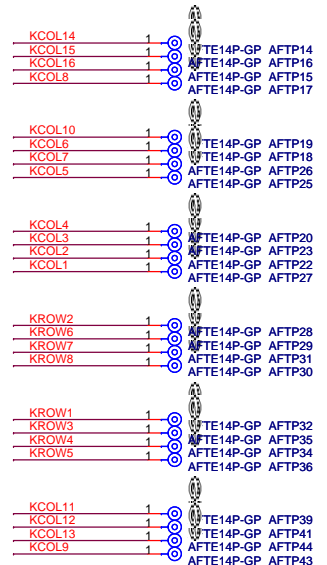
Test Point 放在 Dimm Door 打開可量測處



### Internal Keyboard CONN

CHECK KB SPEC. AND PIN DEFINE

### EMI Bypass cap.



Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

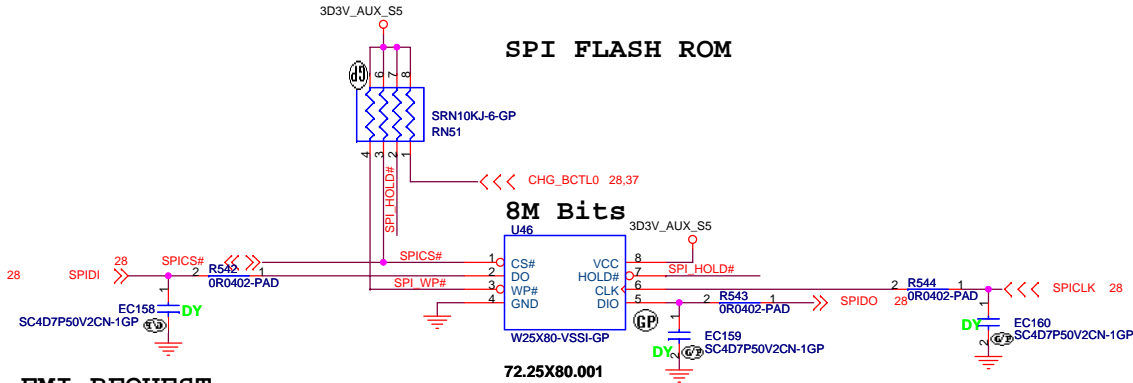
File: **BUTTONS / KB / TOUCHPAD**

Size: Document Number  
Date: Monday, August 18, 2008

Rev: -1  
Yukon

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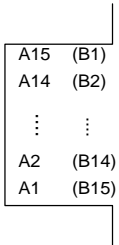
### SPI FLASH ROM



### EMI REQUEST

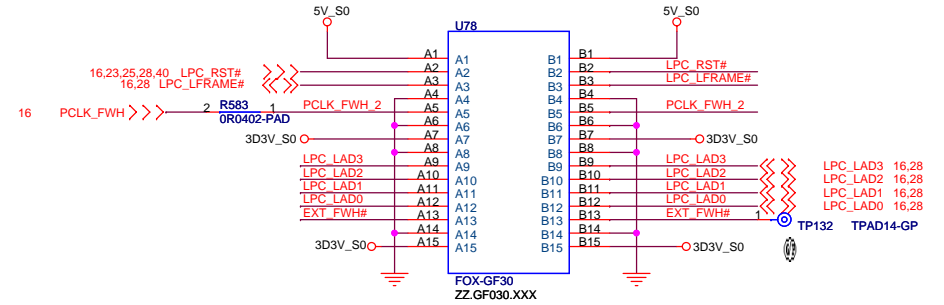
72.25X80.001  
change to 72.25X80.A01

### TOP VIEW

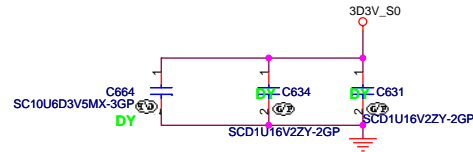


### (BOTTOM VIEW)

### GOLDEN FINGER FOR DEBUG BOARD



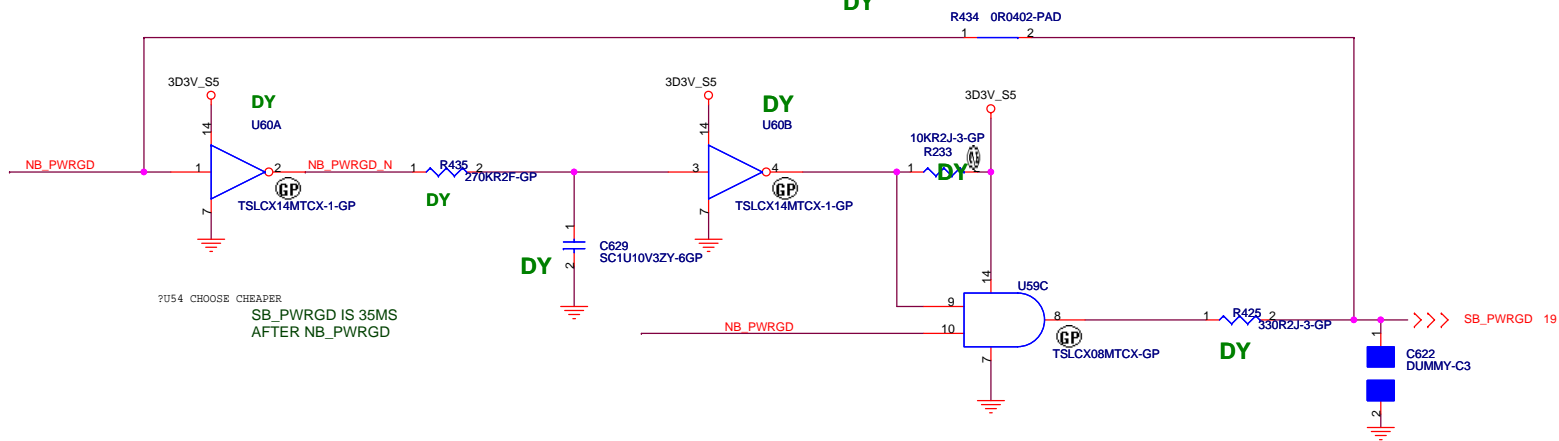
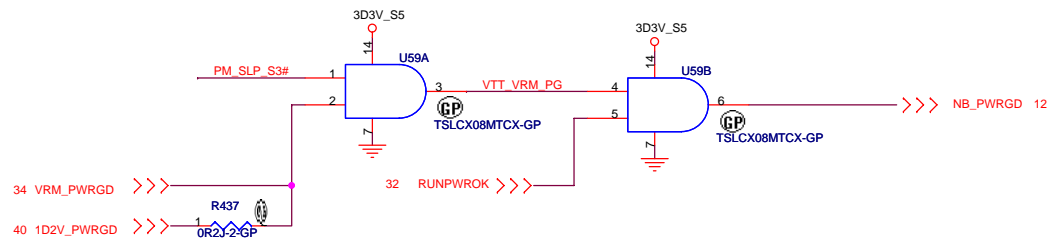
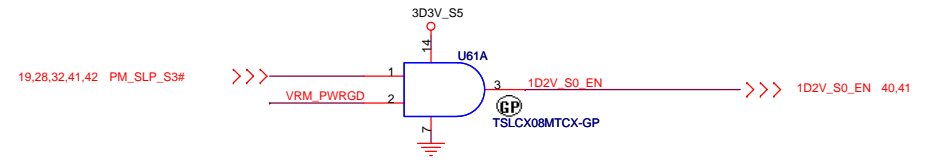
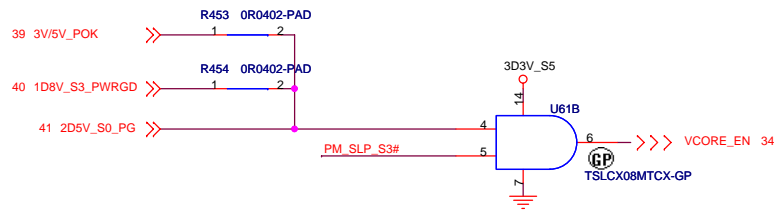
Boot Device must have ID[3:0] = 0000  
Has internal pull-down resistors  
All may be left floated  
FPET7 Elec. P3-46



<Core Design>

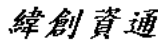
**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			BIOS		
Size	Document Number				Rev
A3	Yukon				-1
Date:	Thursday, August 14, 2008	Sheet	30	of	43



?U54 CHOOSE CHEAPER  
SB\_PWRGD IS 35MS  
AFTER NB\_PWRGD

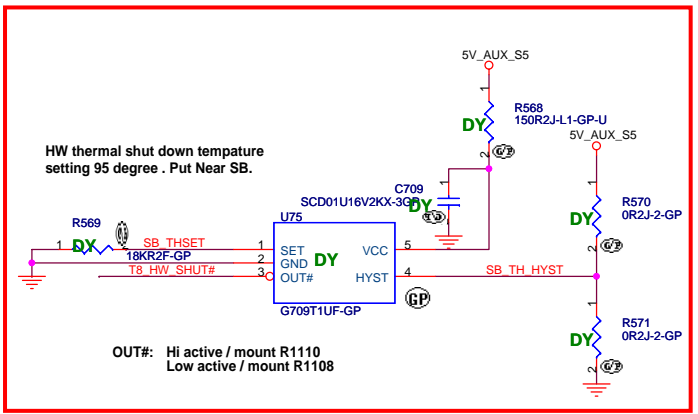
<Core Design>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>POWERGOOD&amp;ENABLES(1/2)</b>	
Size	Document Number
A3	Yukon
Date: Wednesday, August 13, 2008	Sheet 31 of 43
Rev	-1

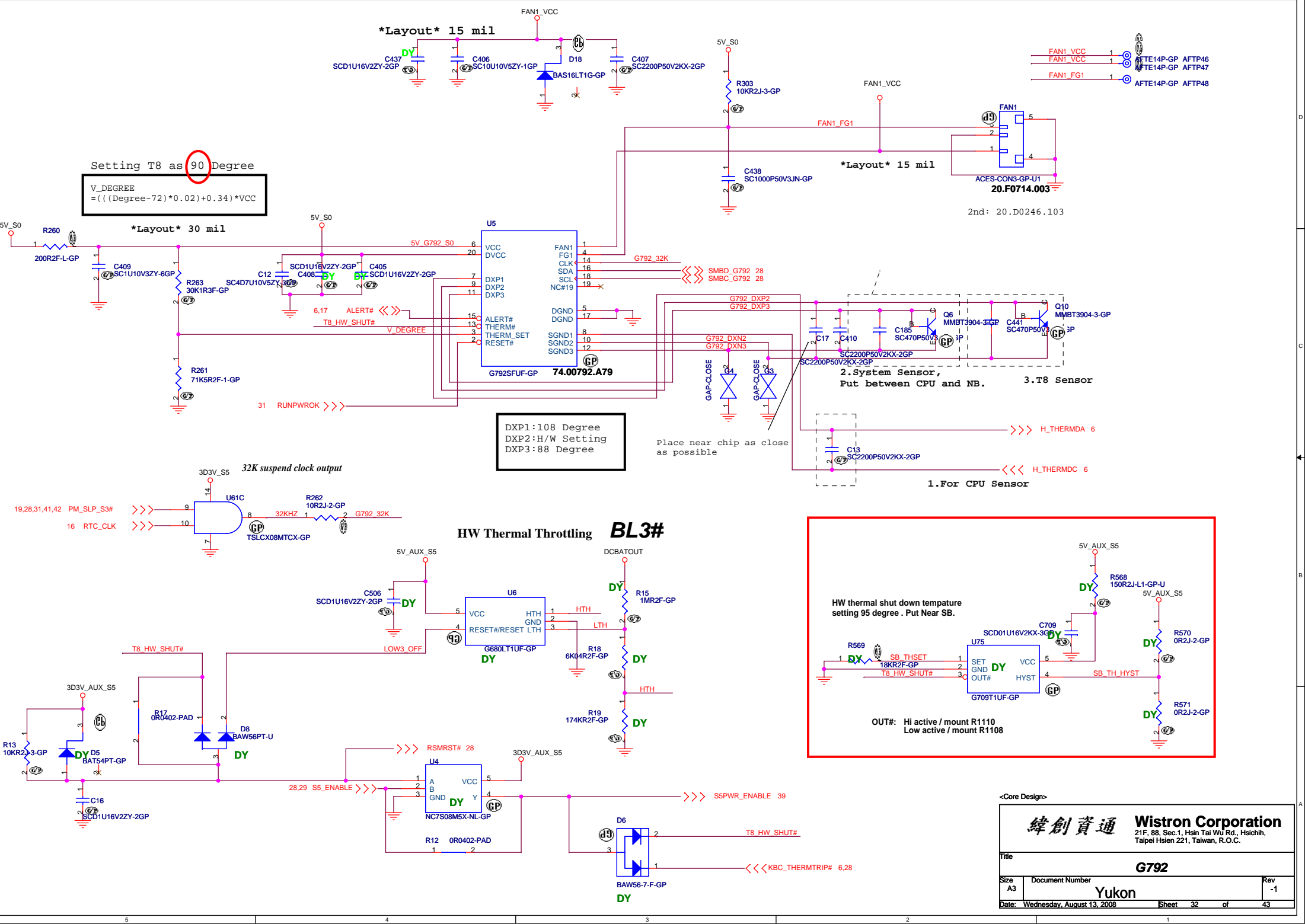
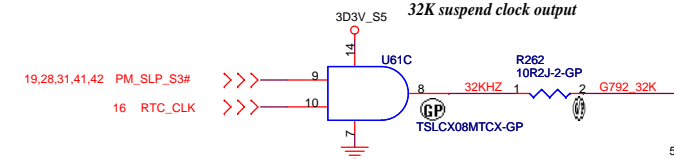
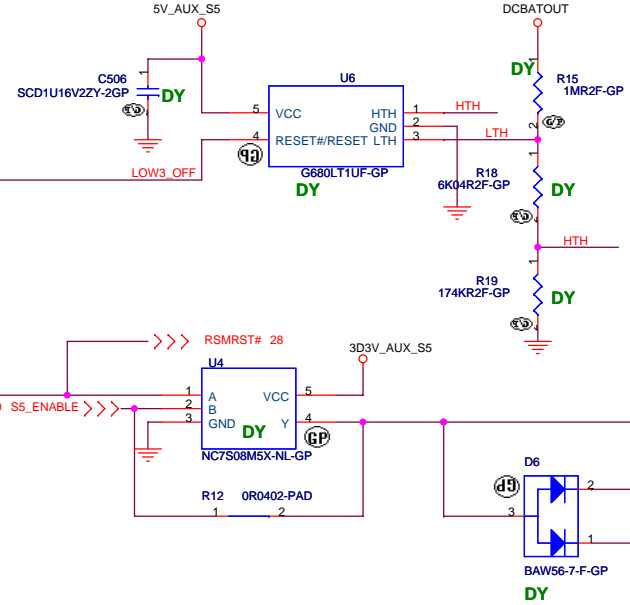
Setting T8 as 90 Degree

$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

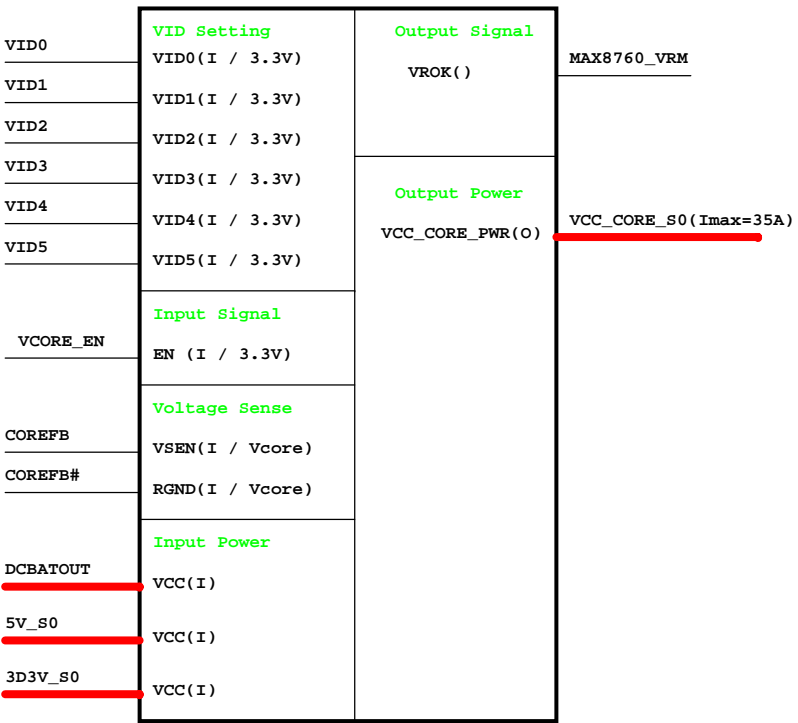


**HW Thermal Throttling BL3#**

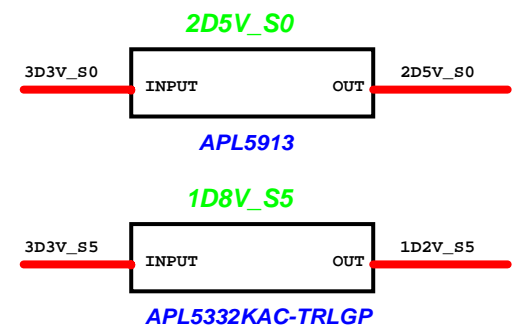
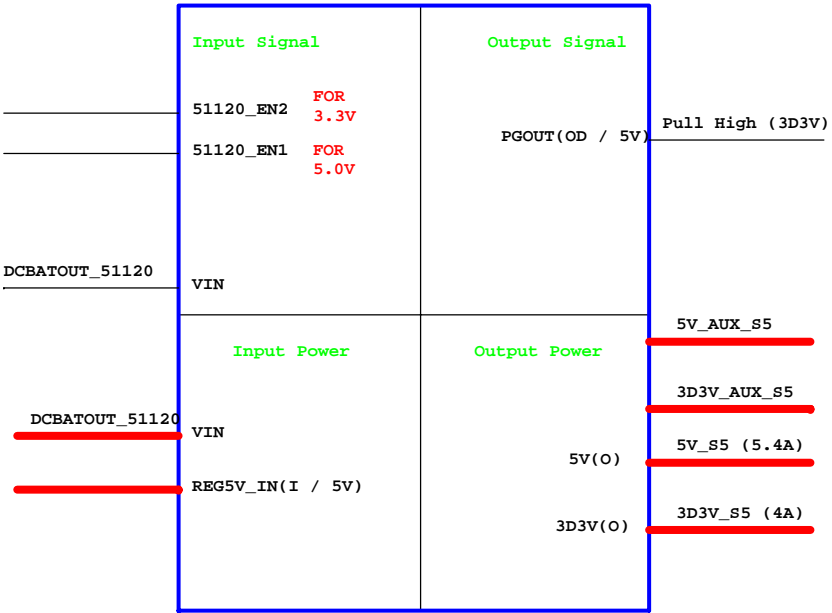




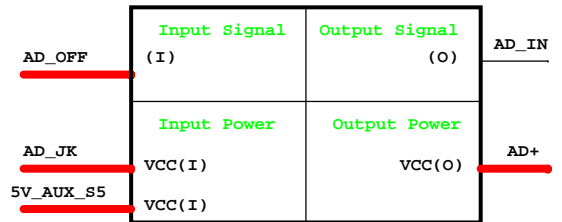
**CPU\_CORE**  
**ISL6264CRZ**



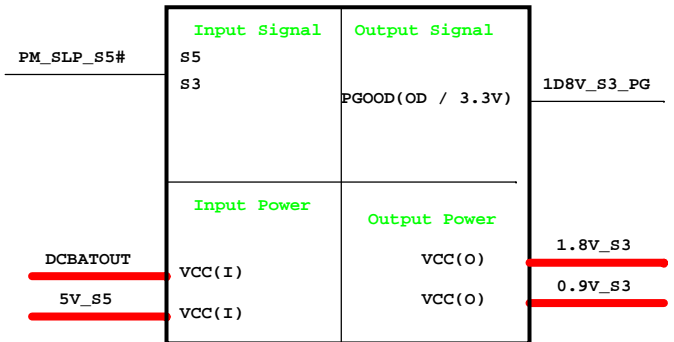
**TI TPS51120**  
**3D3V/5V**



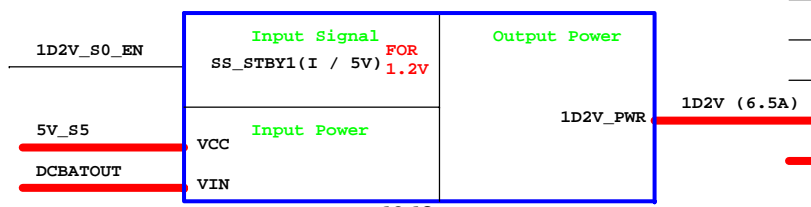
**Adapter**



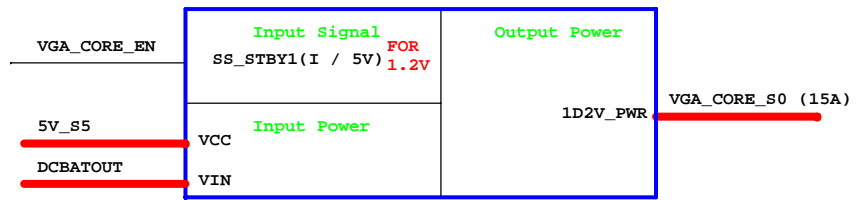
**TI TPS51116**  
**1.8V / 0.9V**



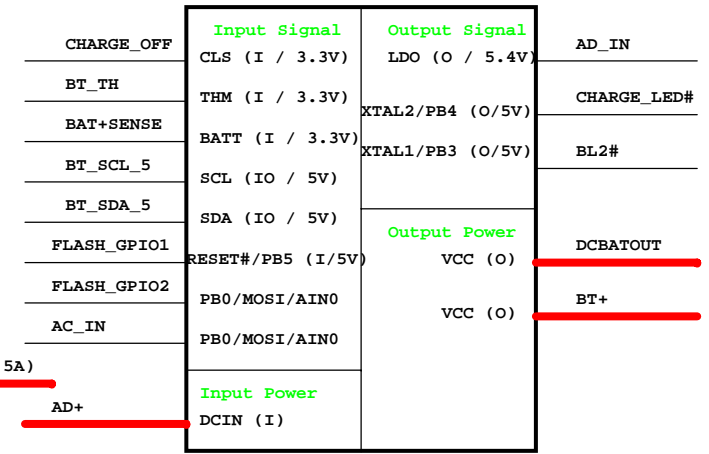
**ISL6268\_1D2V**



**ISL6268\_VGA\_CORE**



**Charger\_ISL6255**



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

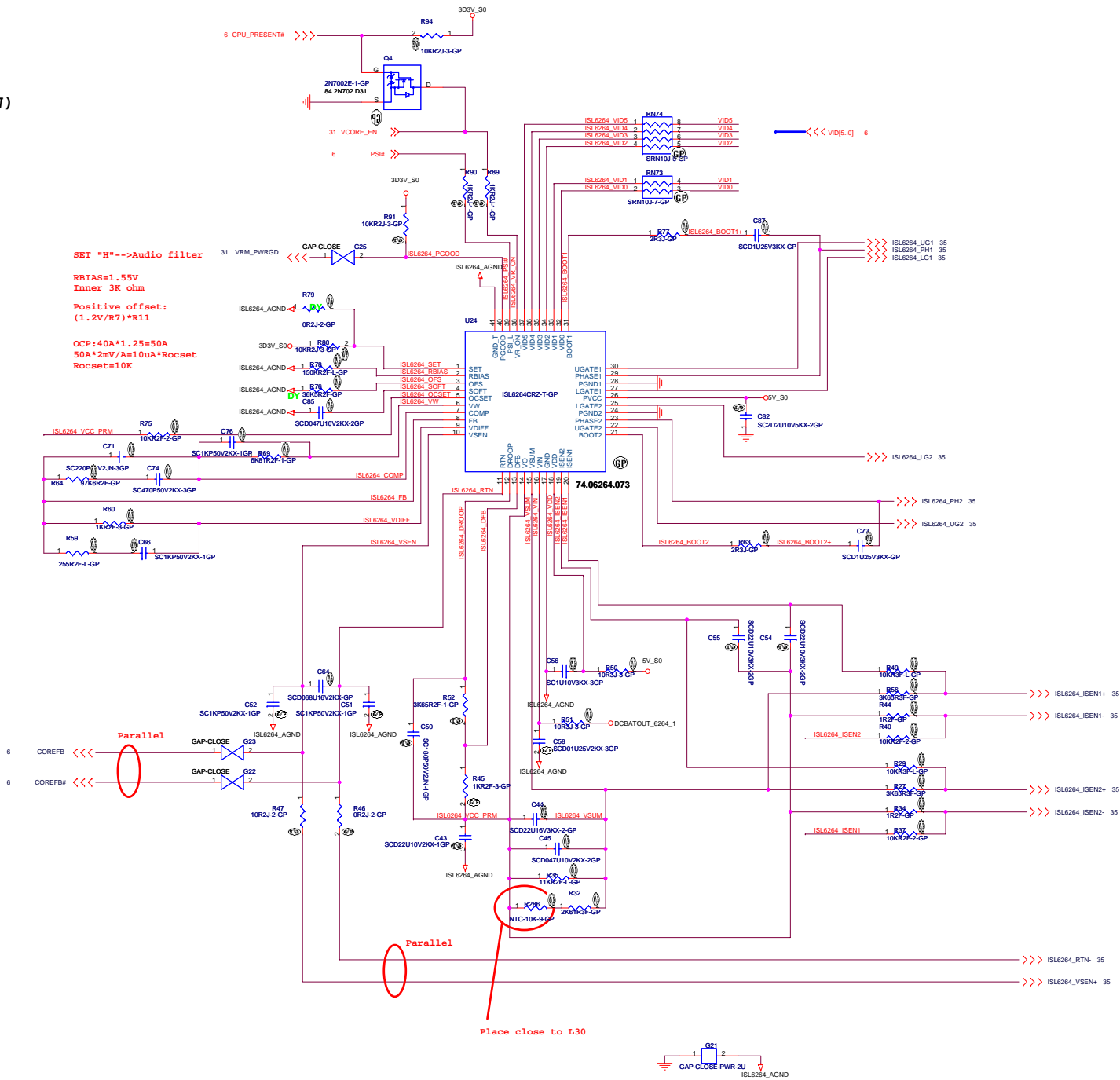
Size: A3 | Document Number: **Yukon** | Rev: **-1**

Date: Wednesday, August 06, 2008 | Sheet: 33 of 43

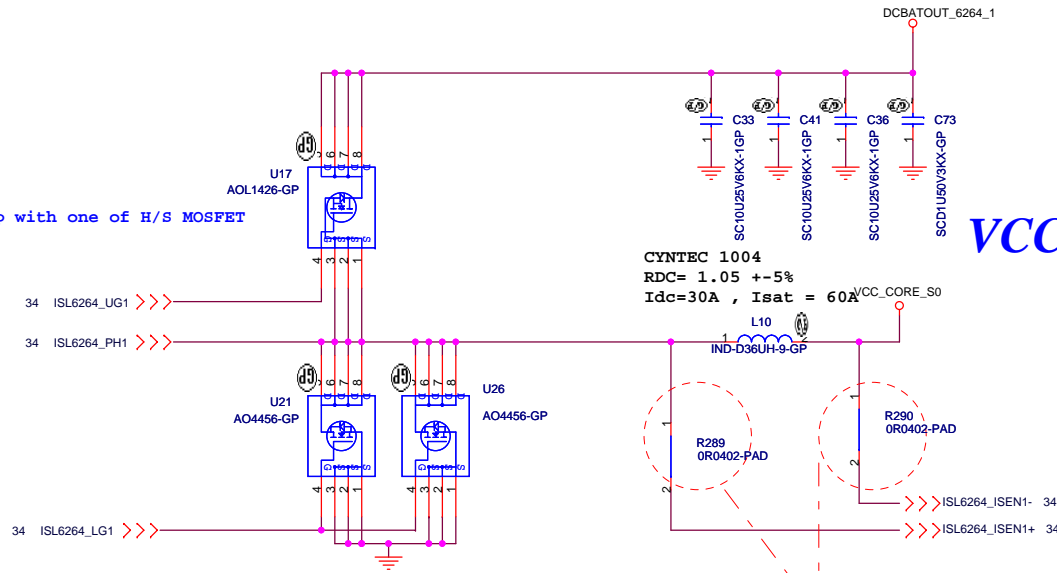
**CPU\_VCORE**  
**VID=1.20V(25W)/1.15V(35W)**  
**I<sub>omax</sub>=21A(25W)/35A(35W)**  
**OCP=40A~45A**

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	0	1	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	1	0	0	0	0	1.175
0	1	0	0	0	1	1.150
0	1	0	0	1	0	1.125
0	1	0	0	1	1	1.100
0	1	0	1	0	0	1.075
0	1	0	1	0	1	1.050
0	1	0	1	1	0	1.025
0	1	0	1	1	1	1.000
0	1	1	0	0	0	0.975
0	1	1	0	0	1	0.950
0	1	1	0	1	0	0.925
0	1	1	0	1	1	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
1	0	0	0	0	0	0.775
1	0	0	0	0	1	0.750
1	0	0	0	1	0	0.725
1	0	0	1	0	0	0.700
1	0	0	1	0	1	0.675
1	0	0	1	1	0	0.650
1	0	0	1	1	1	0.625
1	1	0	0	0	0	0.600
1	1	0	0	0	1	0.575
1	1	0	0	1	0	0.550
1	1	0	0	1	1	0.525
1	1	0	1	0	0	0.500
1	1	0	1	0	1	0.475
1	1	0	1	1	0	0.450
1	1	0	1	1	1	0.425
1	1	1	0	0	0	0.400
1	1	1	0	0	1	0.375



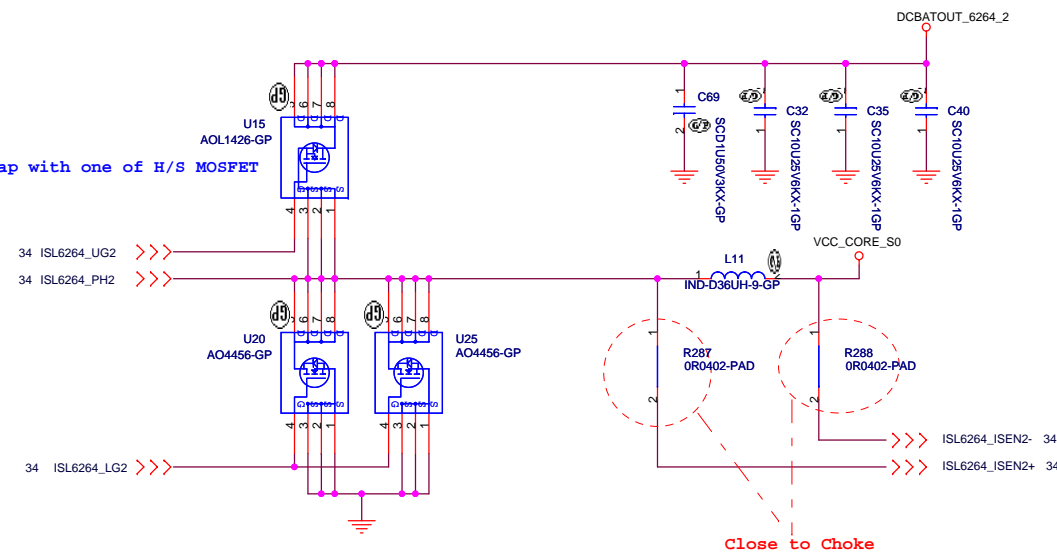
Overlap with one of H/S MOSFET



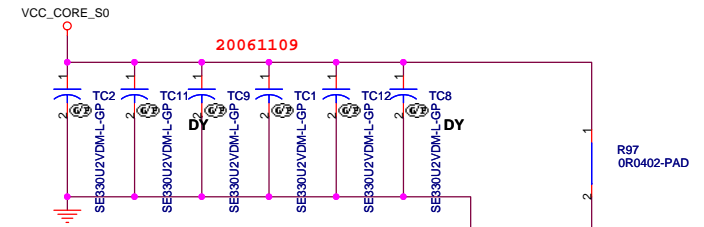
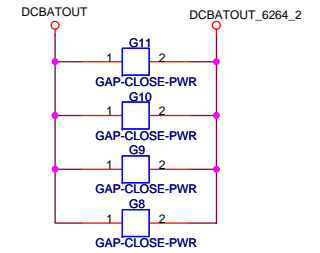
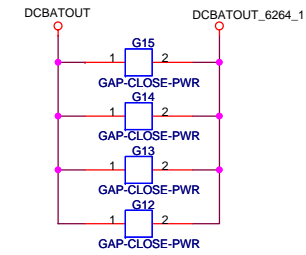
# VCC\_CORE\_S0

Close to Choke

Overlap with one of H/S MOSFET



Close to Choke



Panasonic 330uF / ESR=9mohm

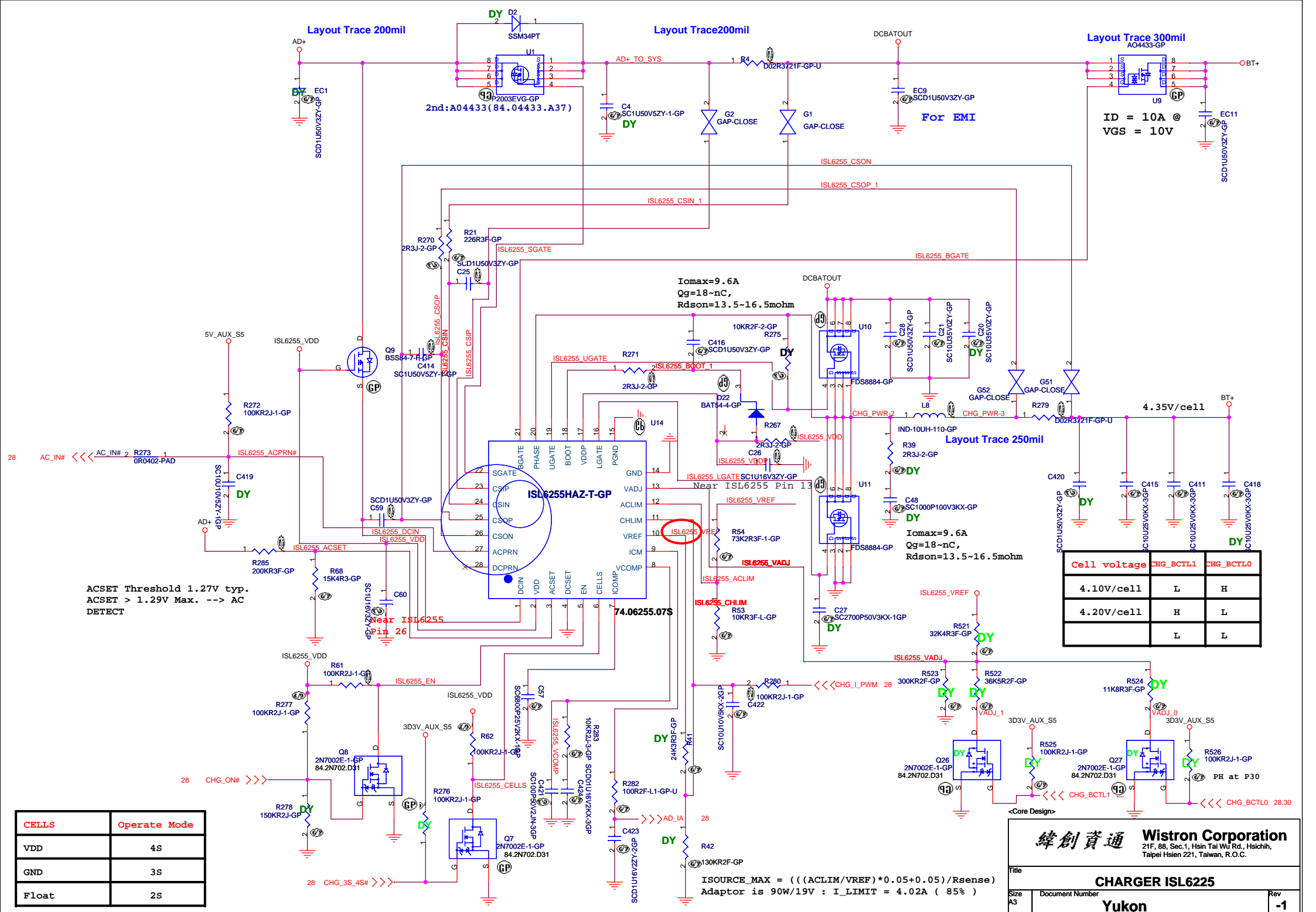
34 ISL6264\_RTN-  
34 ISL6264\_VSEN+

Parallel

<Core Design>

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>CPU Vcore Power_2</b>		
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ACSET Threshold 1.27V typ.  
 ACSET > 1.29V Max. --- AC  
 DETECT

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
	L	L

ISOURCE\_MAX = ((ACLIM/VREF)\*0.05+0.05)/Rsense)  
 Adaptor is 90W/19V : I\_LIMIT = 4.02A ( 85% )

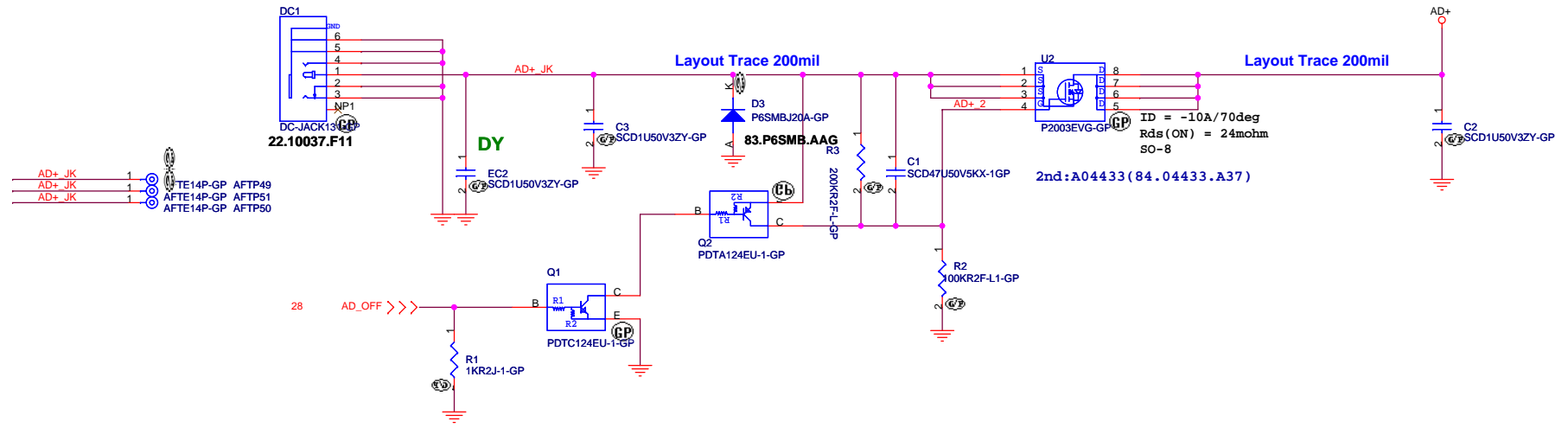
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

**CHARGER ISL6225**

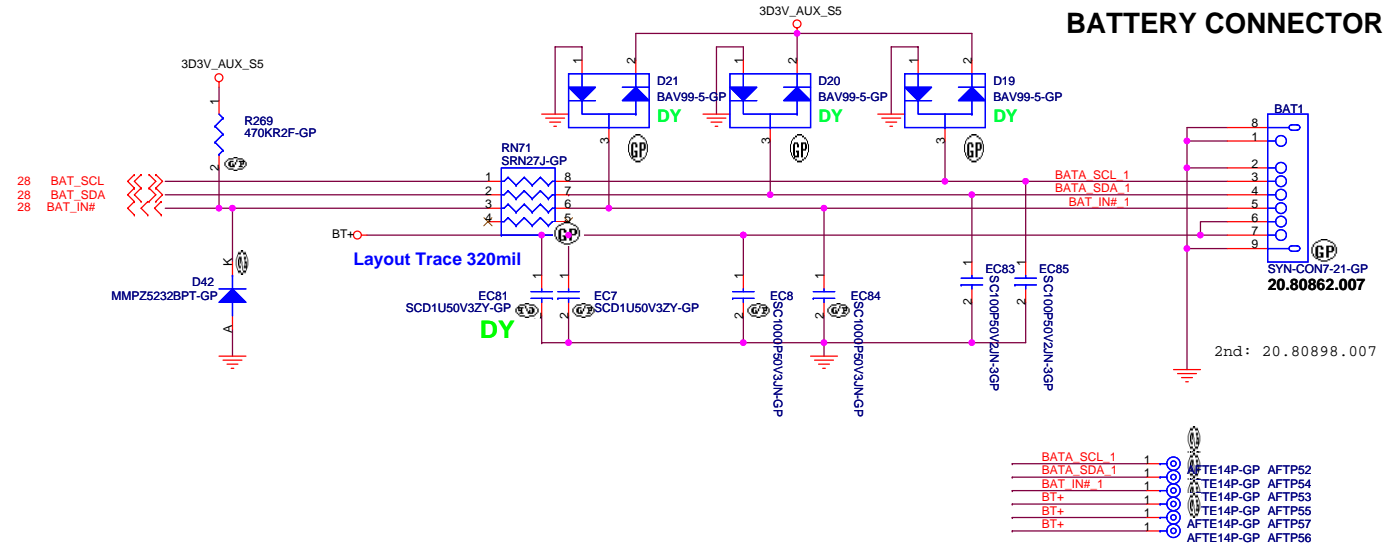
Yukon

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# Adaptor in to generate DCBATOUT

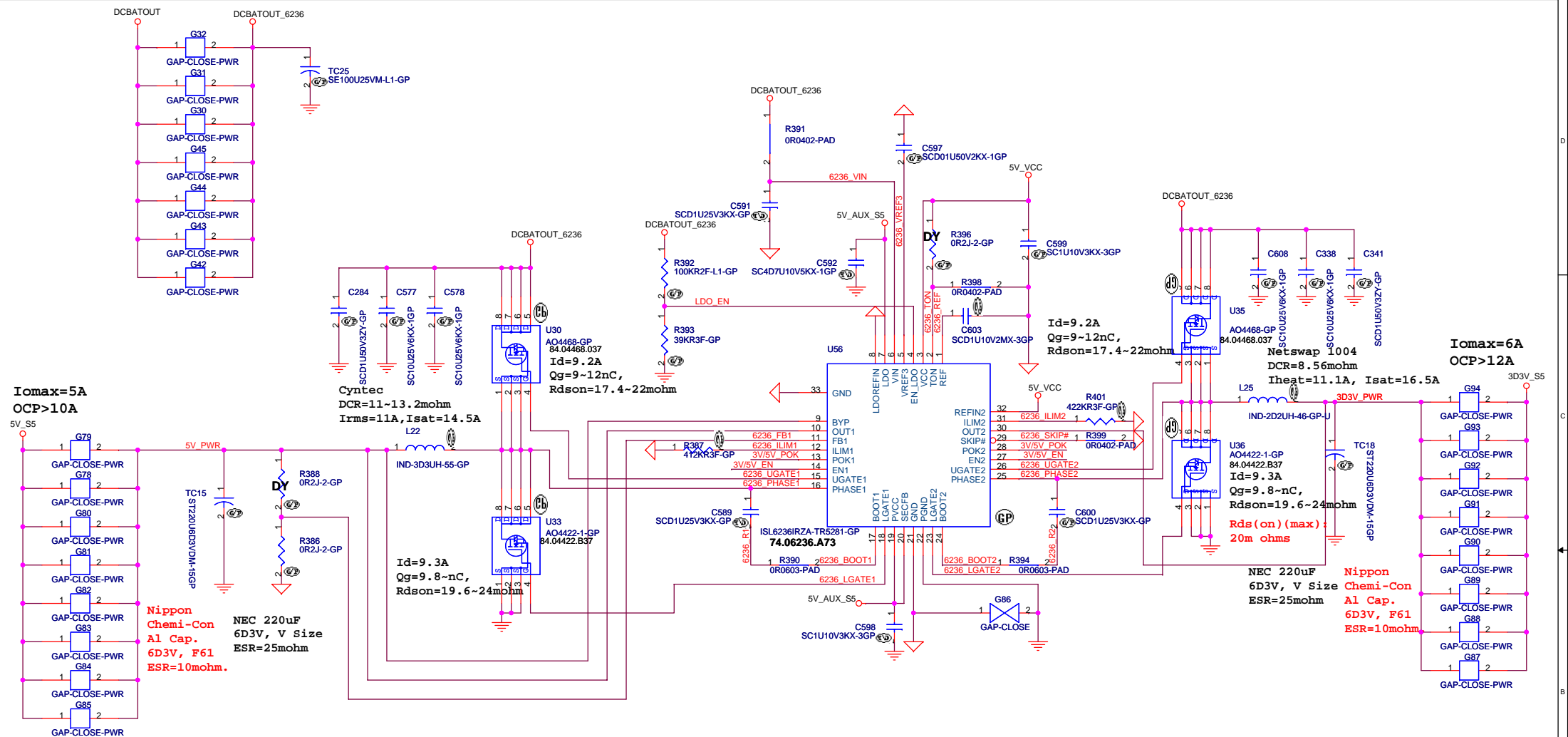


# BATTERY CONNECTOR

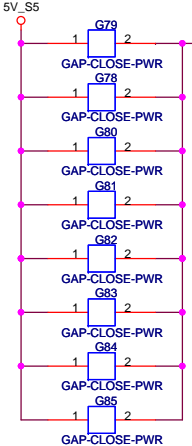


<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>AD/BATT CONN</b>	
Size A3	Document Number <b>Yukon</b>
Date: Friday, August 15, 2008	Rev <b>-1</b>
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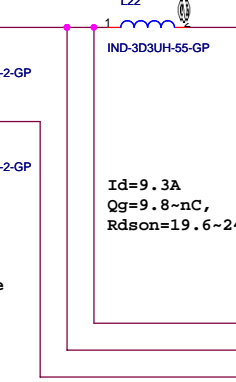
**Iomax=5A**  
OCP>10A



**Nippon Chemi-Con Al Cap.**  
6D3V, F61  
ESR=10mohm.

**NEC 220uF 6D3V, V Size**  
ESR=25mohm

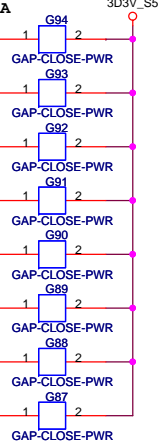
**Cyntec**  
DCR=11~13.2mohm  
Irms=11A, Isat=14.5A



**NEC 220uF 6D3V, V Size**  
ESR=25mohm

**Nippon Chemi-Con Al Cap.**  
6D3V, F61  
ESR=10mohm

**Iomax=6A**  
OCP>12A



**Maximum current: 5A**

If LIR=0.35  
 $\Delta I = 5 \times 0.35 = 1.75A$   
 $V_{in} = 20V; F_{sw} = 400K$   
 $L \sim 3.3\mu H$

**OCP: 5x2=10A**

$I_{ocp} = 10 - (1.75/2) \sim 9.125A$   
 $V_{th} = 9.125A \times 24m\Omega = 219mV$   
 $R(I_{lim}) = (219mV \times 10) / 5\mu A \sim 438K \rightarrow 442K$

**Maximum current: 5A**

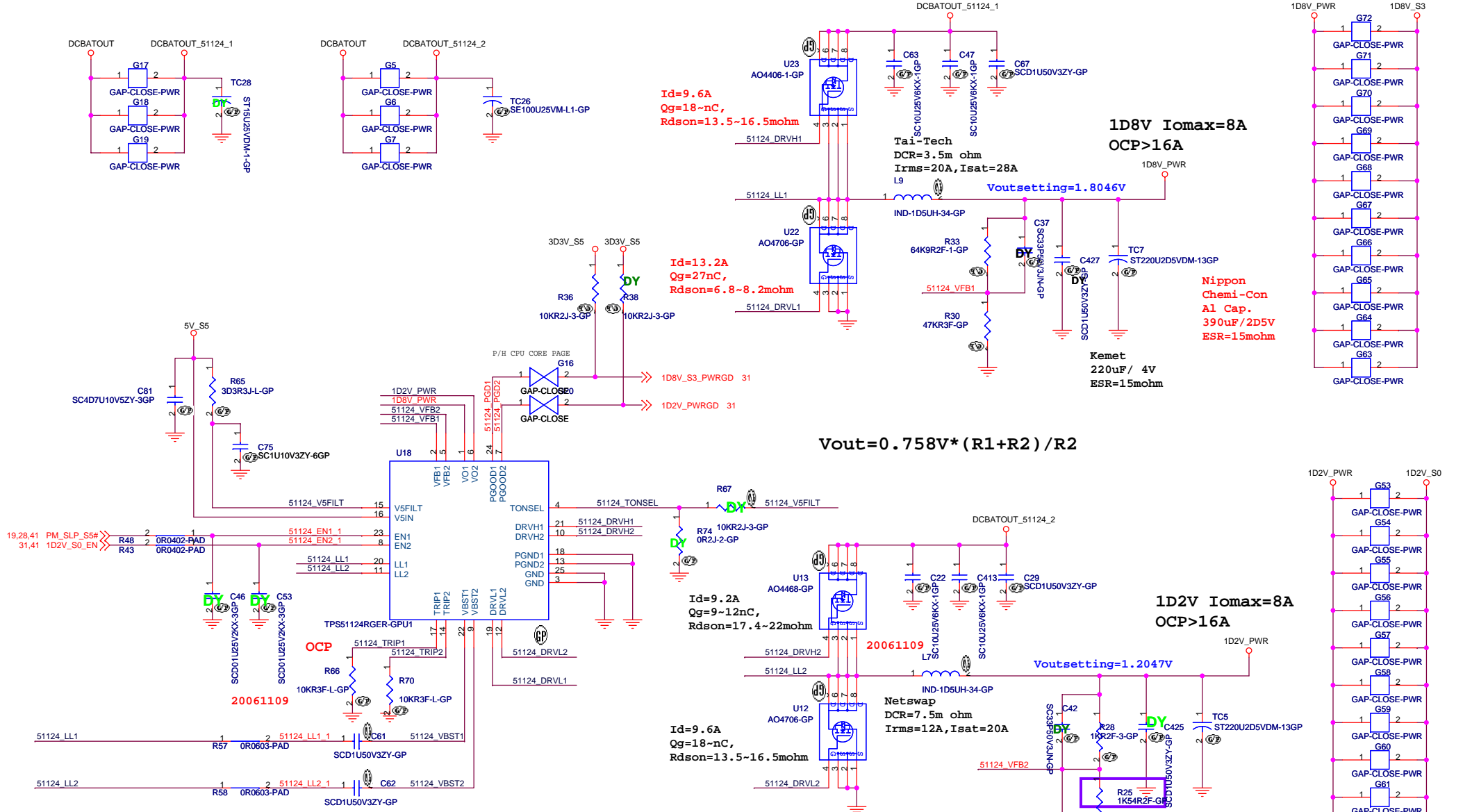
If LIR=0.35  
 $\Delta I = 5 \times 0.35 = 1.75A$   
 $V_{in} = 20V; F_{sw} = 500K$   
 $L \sim 2.2\mu H$

**OCP: 5x2=10A**

$I_{ocp} = 10 - (1.75/2) \sim 9.125A$   
 $V_{th} = 9.125A \times 24m\Omega = 219mV$   
 $R(I_{lim}) = (219mV \times 10) / 5\mu A \sim 438K \rightarrow 442K$

<Core Design>

<b>緯創資通 Wistron Corporation</b>	
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<b>ISL6236 5V 3D3V</b>	
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<b>Yukon</b>	
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**Vtrip(mV)=Rtrip(Kohm)\*10(uA)**  
**Iocp=(Vtrip/Rdson)+((1/(2\*L\*f))\*((Vin-Vout)\*Vout)/Vin))**

	GND	OPEN	V5FILT
<b>TONSEL</b>	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

STRP_DATA	1D2V(VCC_NB)
0	1.0
1	1.2

<Core Design>

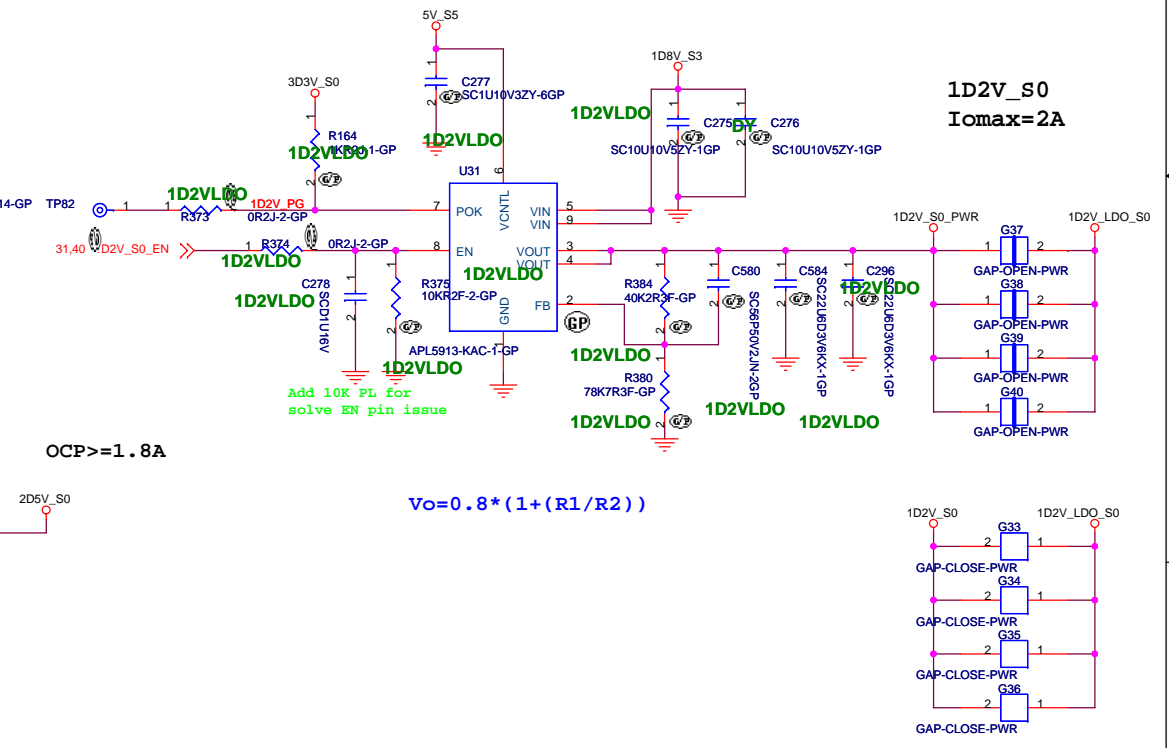
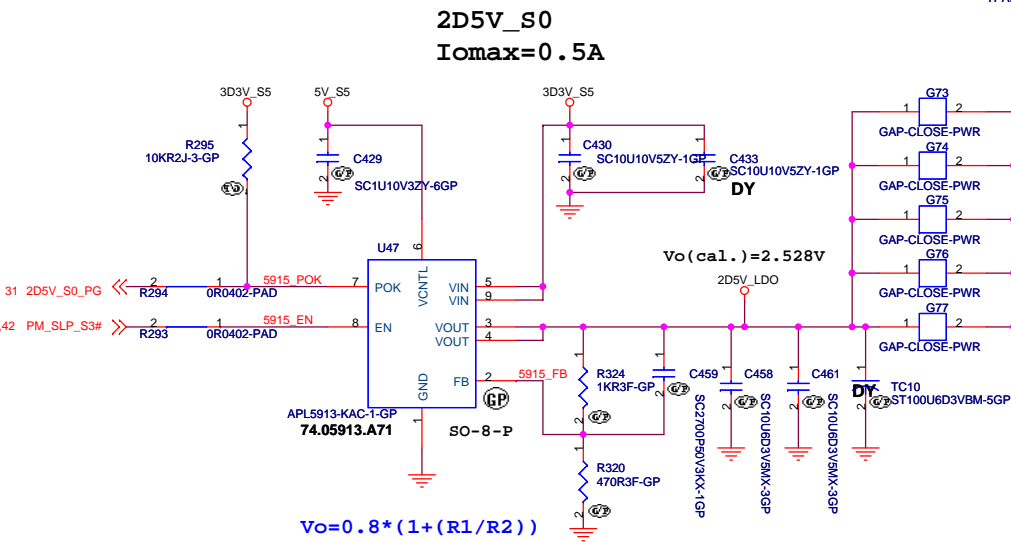
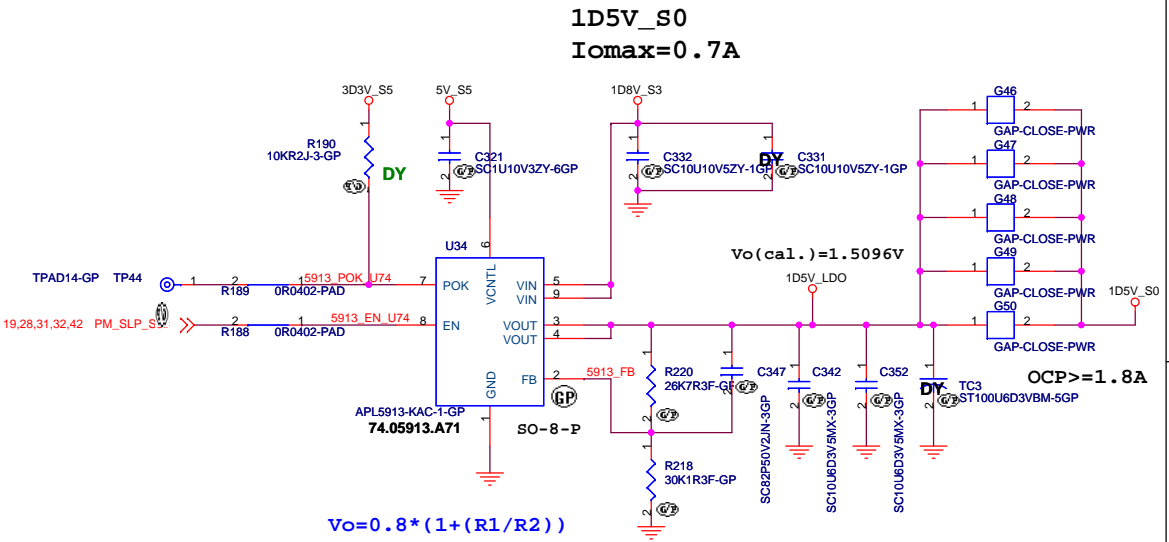
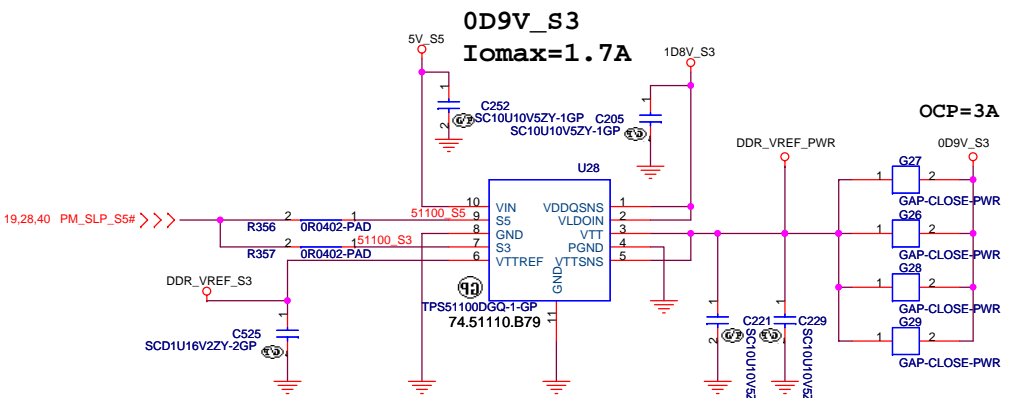
**緯創資通 Wistron Corporation**  
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Title: **TPS51124 1D8V 1D2V**

Size A3 Document Number **Yukon** Rev **-1**

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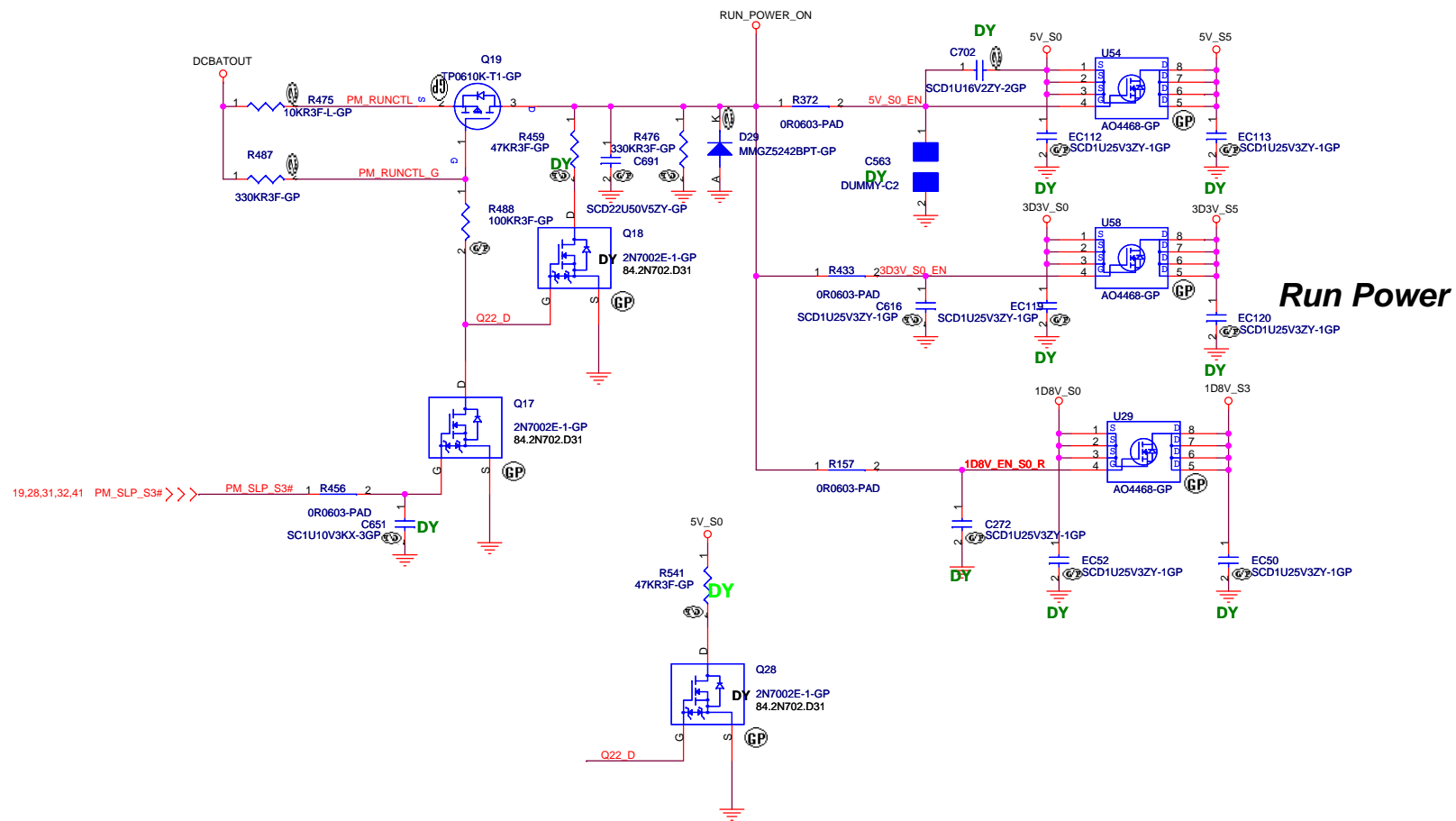
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**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

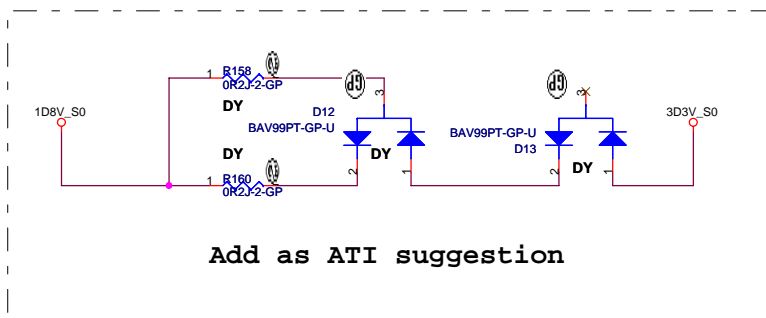
Title: **2D5V/1D5V/0D9V**

Size: A3 Document Number: **Yukon** Rev: **-1**

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### Run Power



Add as ATI suggestion

### Power On Logic

<Core Design>

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Title: <b>RUB POWER</b>		
Size: A3	Document Number: Yukon	Rev: -1
Date: Wednesday, August 06, 2008	Sheet: 42	of: 43



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