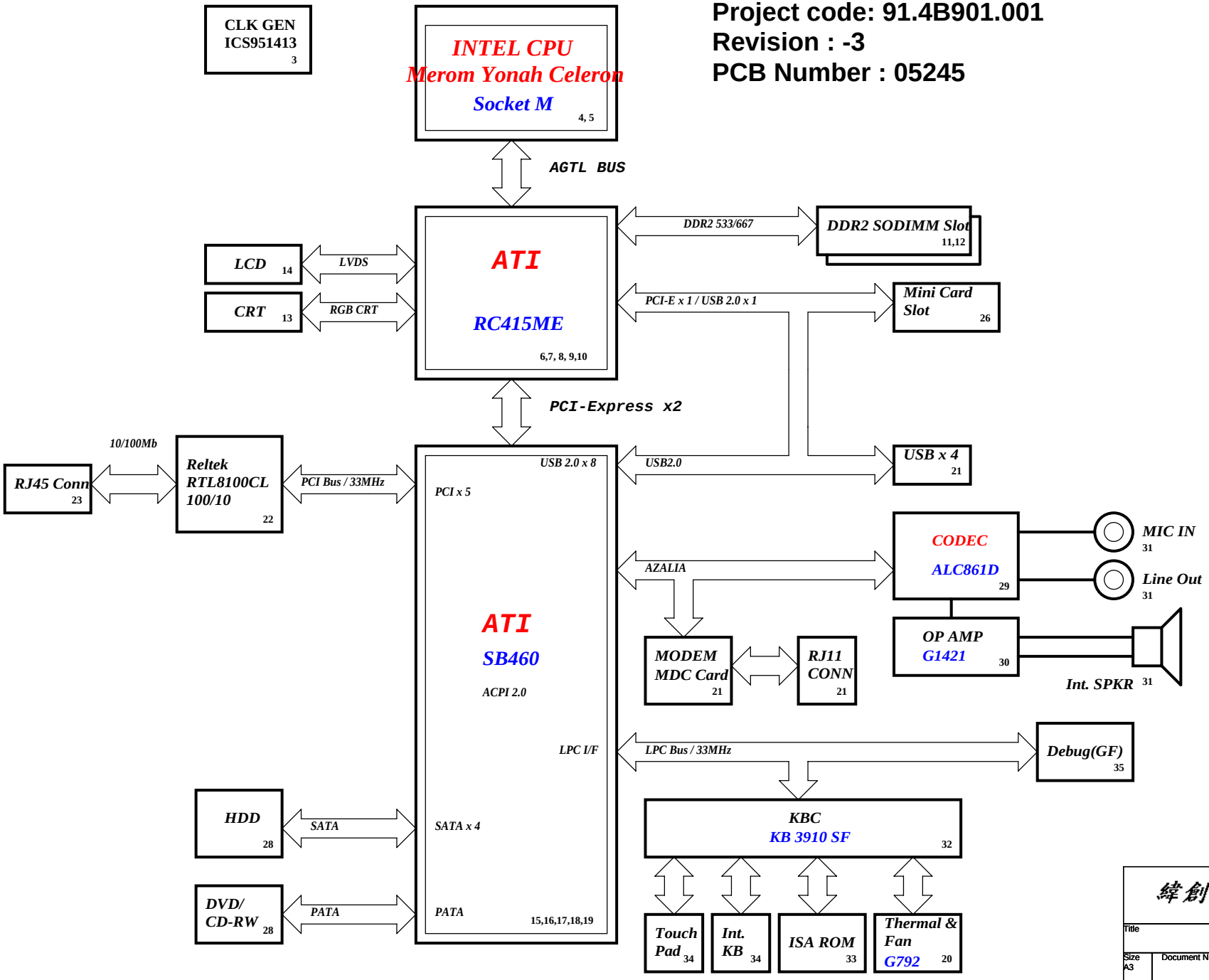
Y4A Block Diagram

Project code: 91.4B901.001
Revision : -3
PCB Number : 05245



SYSTEM DC/DC	
MAX8734 42, 43	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5, 5V_S5
TPS51116 41	
DCBATOUT	1D8V_S3 0D9V_S0
APL5913 44	
3D3V_S0	1D05V_S0 1D5V_S0
APL5912	
1D8V_S3	1D2V_S0

CHARGER	
MAX1909 45	
INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC	
ISL6262 39,40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.84~1.6V 30A

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Title	**BLOCK DIAGRAM**	
Size A3	Document Number Y4A	Rev -1
Date: Tuesday, January 23, 2007	Sheet 1 of 49	

HISTORY

Y4A PCI Routing

	IRQ	IDSEL	REQ/GNT	Device No.	REMARK
RTL8100CL	INT_PIRQH#	PCI_AD23	PCI_GNT#2/REQ#2	7	
R5C832	INT_PIRQE# INT_PIRQG# INT_SERIRQ	PCI_AD17	PCI_GNT#0/REQ#0	1	INTA# CARD READER INTB# IEEE1394

PCB STACK

TOP

VCC

IN1

IN2

GND

BOTTOM

POWER PLANE

CPU
VCC_CORE__S0,
1D5V_S0,
1D05V_S0

NB
1D2V_S0,
1D8V_S0,
1D05_S0

SB
1D8V_S0,
3D3V_SB_S0,
3D3V_SB_S5,
5V_S0

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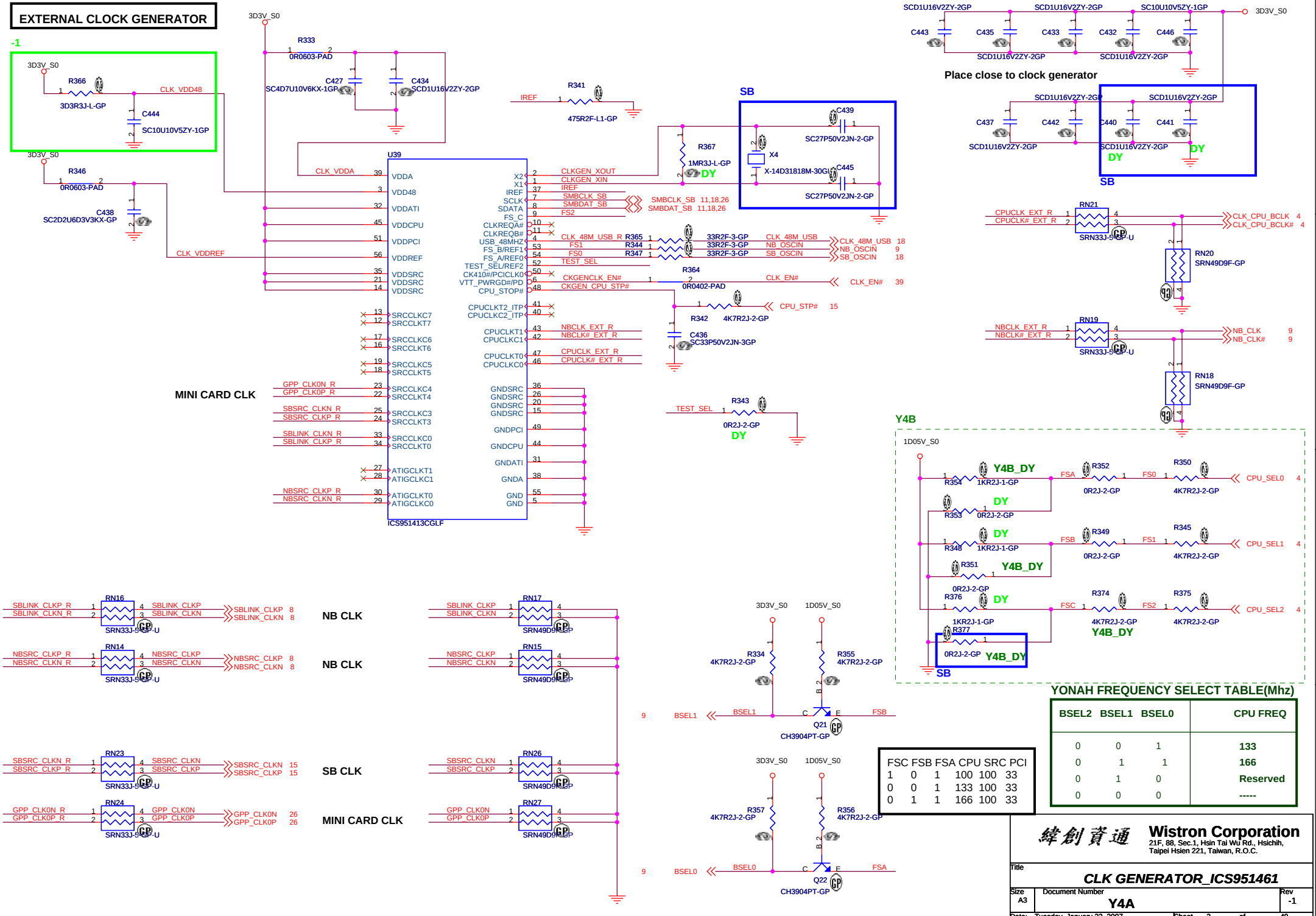
Title: HISTORY

Size: Custom | Document Number: Y4A | Rev: -1

Date: Tuesday, January 23, 2007 | Sheet 2 of 49

EXTERNAL CLOCK GENERATOR



YONAH FREQUENCY SELECT TABLE(Mhz)

BSEL2	BSEL1	BSEL0	CPU FREQ
0	0	1	133
0	1	1	166
0	1	0	Reserved
0	0	0	-----

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33

緯創資通
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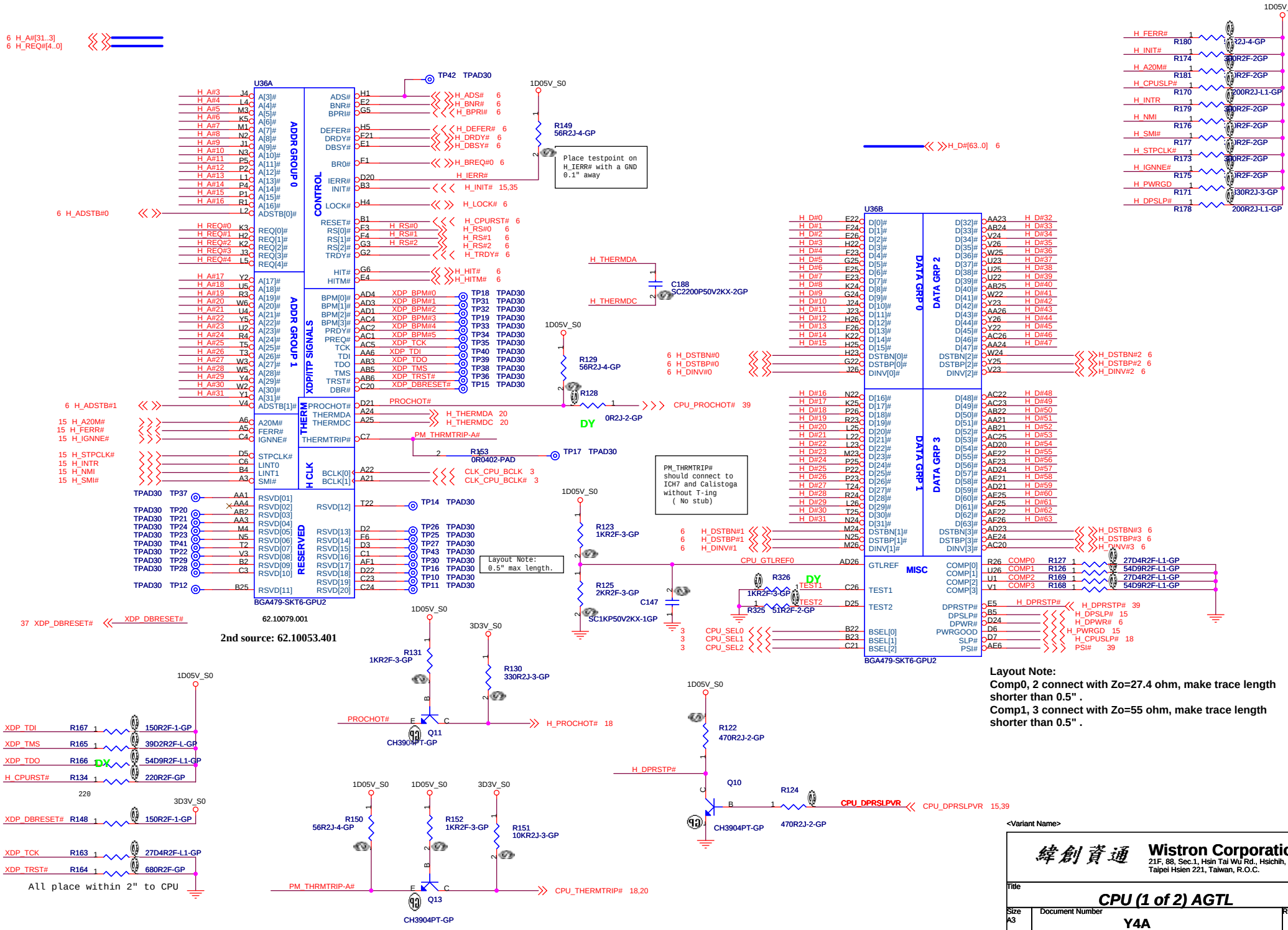
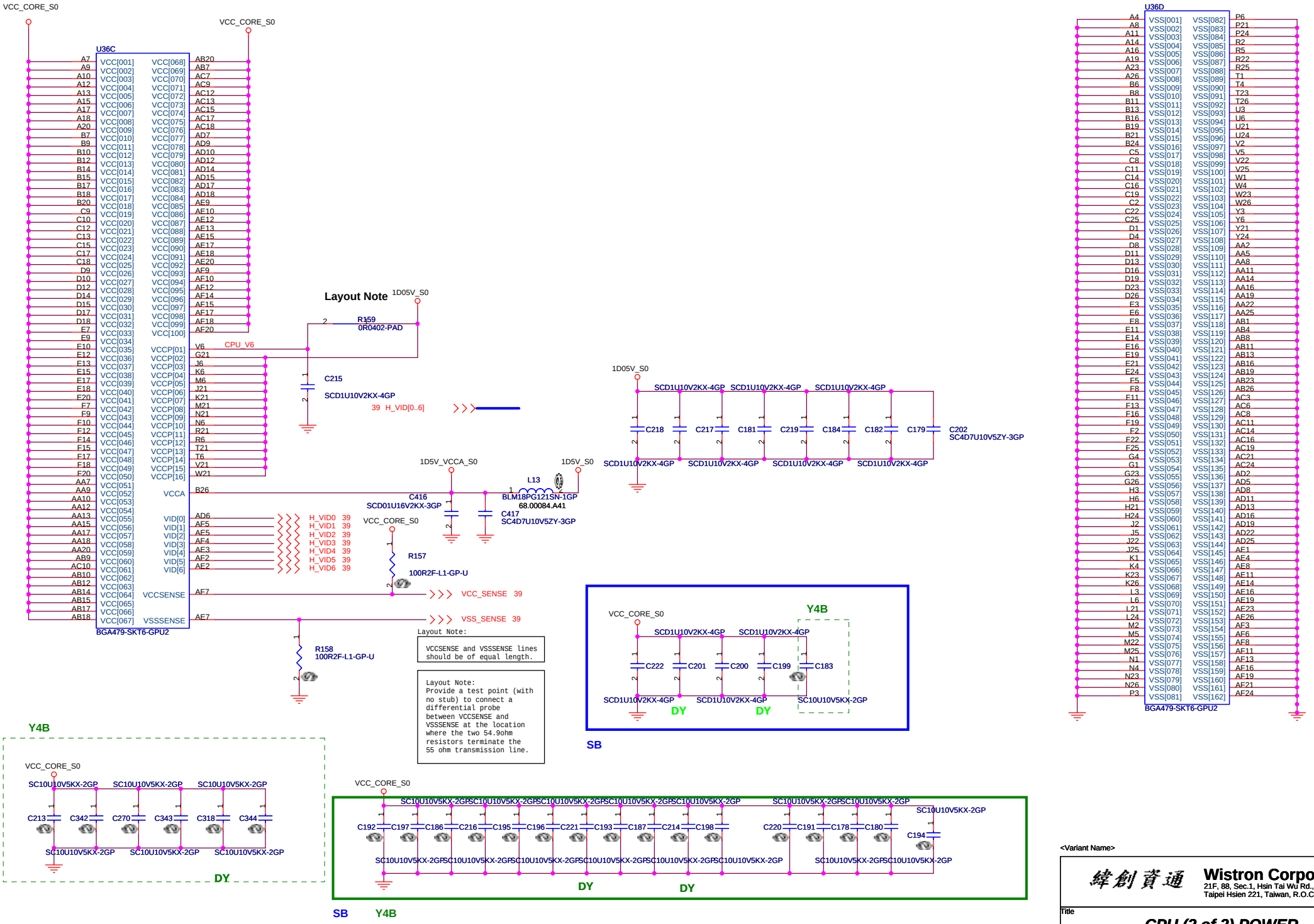
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLK GENERATOR_ICS951461**

Size: A3 | Document Number: Y4A | Rev: -1

Date: Tuesday, January 23, 2007 | Sheet 3 of 49


6 H_A#[31..3]
6 H_REQ#[4..0]
U36A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
BGA479-SKT6-GPU2
62.10079.001
2nd source: 62.10053.401
TP42 TPAD30
1D05V_S0
R149 56R2J-4-GP
Place testpoint on H_IERR# with a GND 0.1" away
H_ADSTB#0
H_ADSTB#1
H_THERMDA
H_THERMDC
C188 SC2200P50V2KX-2GP
R129 56R2J-4-GP
R128 0R2J-2-GP
DY
CPU_PROCHOT# 39
R153 0R0402-PAD
TP17 TPAD30
PM_THRMTRIP# should connect to ICH7 and Calistoga without T-ing (No stub)
Layout Note: 0.5" max length.
XDP_DBRESET#
U36B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
BGA479-SKT6-GPU2
H_D#[63..0] 6
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
H_DINV#2
H_DSTBN#3
H_DSTBP#3
H_DINV#3
CPU_GTLREF0
R123 1KR2F-3-GP
R125 2KR2F-3-GP
C147 SC1KP50V2KX-1GP
R326 1KR2F-3-GP
R325 51R2F-2-GP
CPU_SEL0
CPU_SEL1
CPU_SEL2
R26 COMP0 R127 27D4R2F-L1-GP
U26 COMP1 R126 54D9R2F-L1-GP
U1 COMP2 R169 27D4R2F-L1-GP
V1 COMP3 R168 54D9R2F-L1-GP
H_DPRSTP# 39
H_DPSLP# 15
H_DPWR# 6
H_PWRGD 15
H_CPUSLP# 18
PSI# 39
H_FERR# R180 200R2J-4-GP
H_INIT# R174 330R2F-2GP
H_A20M# R181 330R2F-2GP
H_CPUSLP# R170 200R2J-L1-GP
H_INTR R179 330R2F-2GP
H_NMI R176 330R2F-2GP
H_SMI# R177 330R2F-2GP
H_STPCLK# R173 330R2F-2GP
H_IGNNE# R175 330R2F-2GP
H_PWRGD R171 330R2J-3-GP
H_DPSLP# R178 200R2J-L1-GP
XDP_TDI R167 150R2F-1-GP
XDP_TMS R165 39D2R2F-L-GP
XDP_TDO R166 54D9R2F-L1-GP
H_CPURST# R134 220R2F-GP
220
XDP_DBRESET# R148 150R2F-1-GP
XDP_TCK R163 27D4R2F-L1-GP
XDP_TRST# R164 680R2F-GP
All place within 2" to CPU
R131 1KR2F-3-GP
R130 330R2J-3-GP
PROCHOT#
Q11 CH3904PT-GP
H_PROCHOT# 18
R122 470R2J-2-GP
H_DPRSTP#
Q10 CH3904PT-GP
R124 470R2J-2-GP
CPU_DPRSLPVR
CPU_DPRSLPVR 15,39
R150 56R2J-4-GP
R152 1KR2F-3-GP
R151 10KR2J-3-GP
PM_THRMTRIP-A#
Q13 CH3904PT-GP
CPU_THERMTRIP# 18,20
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (1 of 2) AGTL
Size A3
Document Number Y4A
Rev -1
Date: Tuesday, January 23, 2007
Sheet 4 of 49


VCC_CORE_S0
U36C
BGA479-SKT6-GPU2
Layout Note
1D05V_S0
R159
0R0402-PAD
CPU_V6
C215
SCD01U16V2KX-3GP
39 H_VID[0..6]
1D05V_VCCA_S0
L13
BLM18PG121SN-1GP
68.00084.A41
C416
C417
SC4D7U10V5ZY-3GP
R157
100R2F-L1-GP-U
VCC_SENSE 39
VSS_SENSE 39
R158
100R2F-L1-GP-U
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
SCD1U10V2KX-4GP
C218
C217
C181
C219
C184
C182
C179
C202
SC4D7U10V5ZY-3GP
Y4B
DY
SB
C222
C201
C200
C199
C183
SC10U10V5KX-2GP
C213
C342
C270
C343
C318
C344
C192
C197
C186
C216
C195
C196
C221
C193
C187
C214
C198
C220
C191
C178
C180
C194
U36D
BGA479-SKT6-GPU2
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2) POWER
Size
A3
Document Number
Y4A
Rev
-1
Date: Tuesday, January 23, 2007
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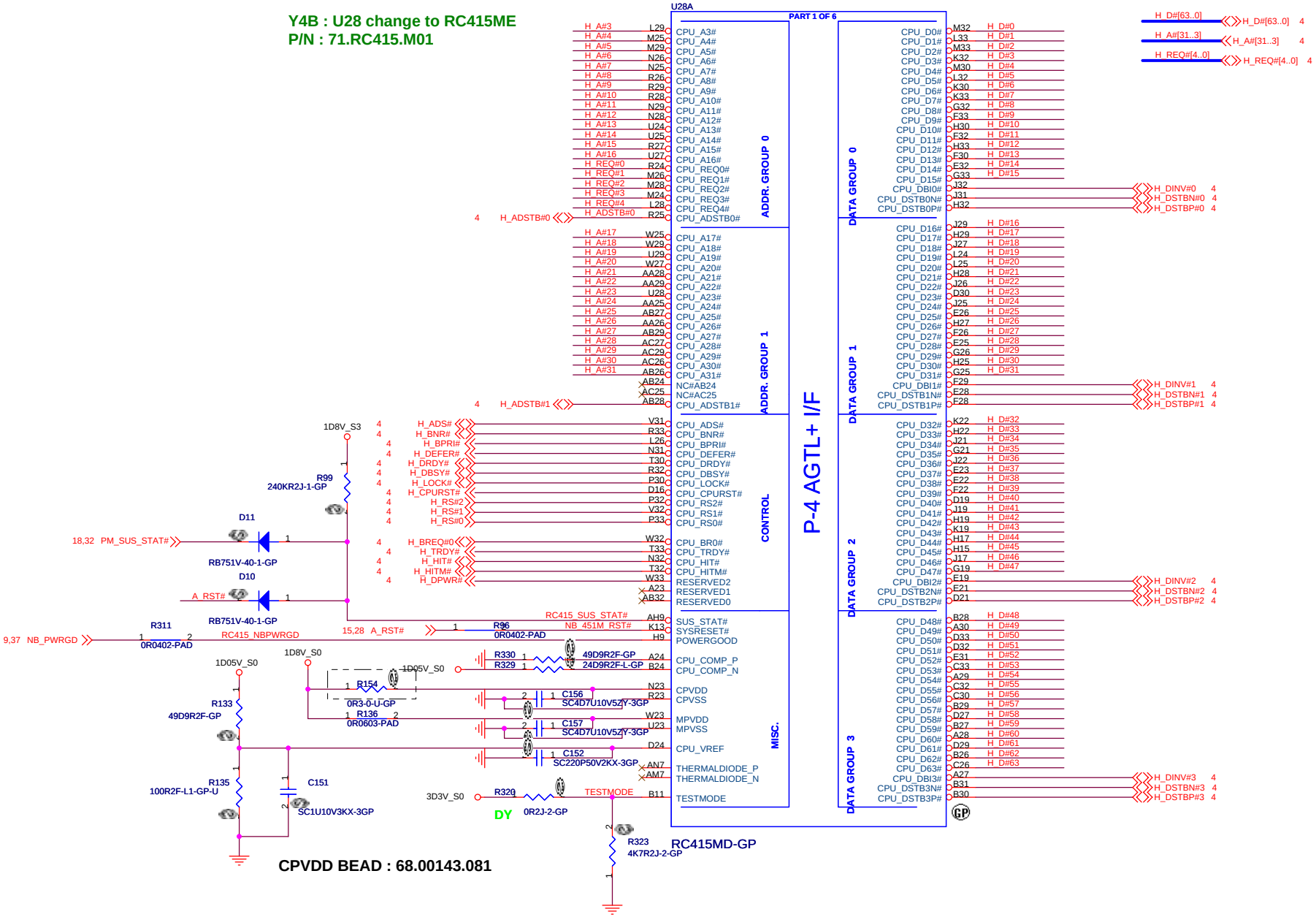
Y4B : U28 change to RC415ME
P/N : 71.RC415.M01



CPVDD BEAD : 68.00143.081

TESTMODE	NB MODE
LOW	NORMAL MODE
HIGH	TEST MODE

緯創資通 **Wistron Corporation**
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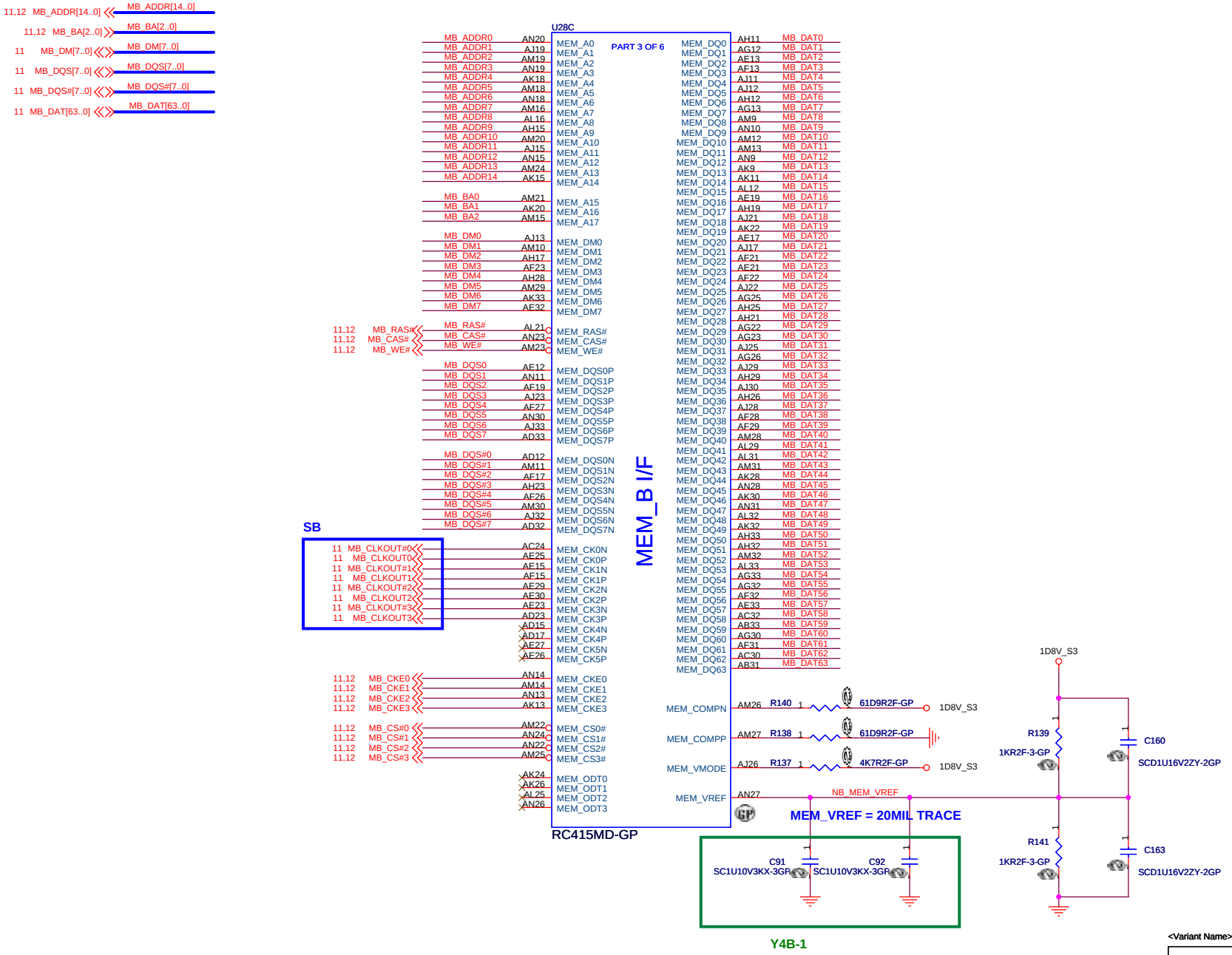
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RC415MD (1 of 5) AGTL**

Size	Document Number	Rev
A3	Y4A	-1

Date: Tuesday, January 23, 2007 Sheet 6 of 49



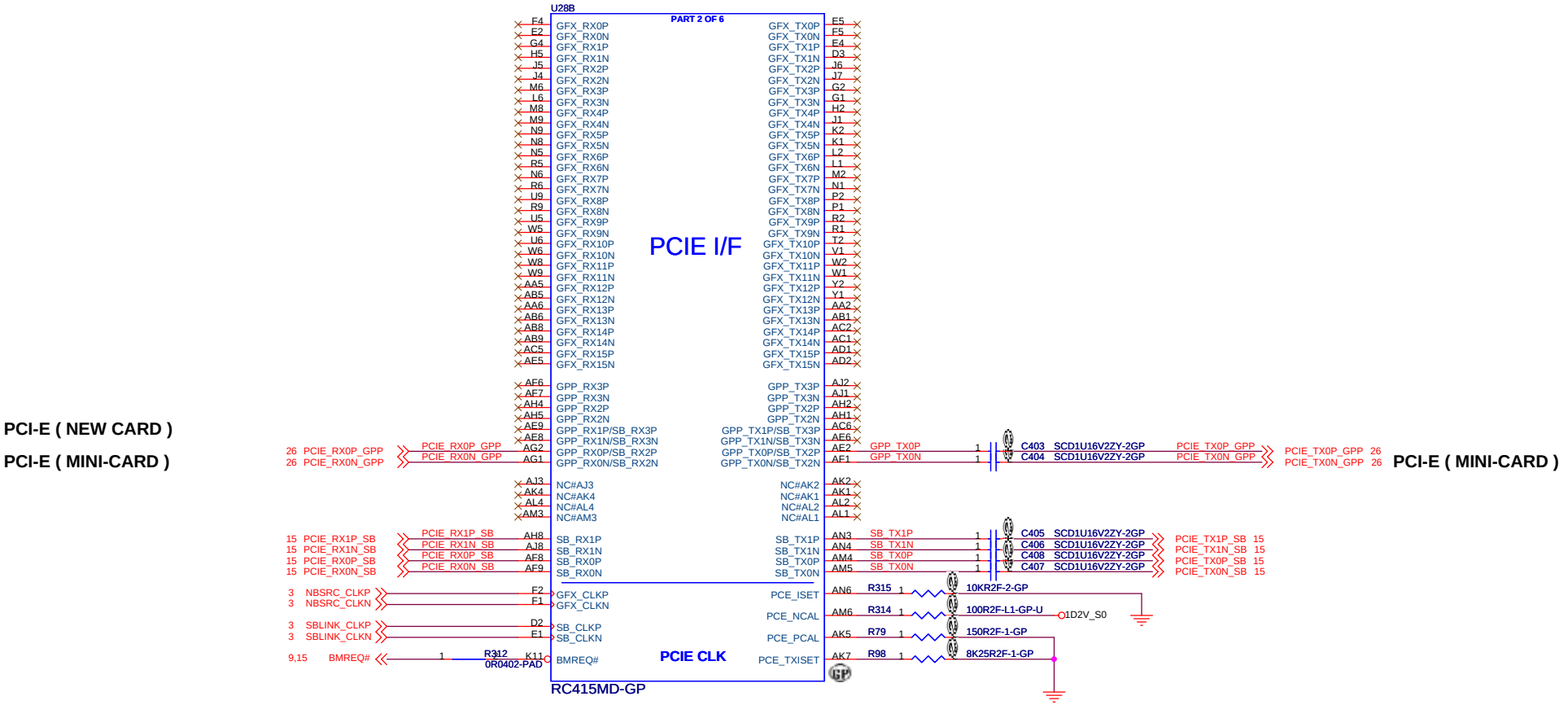
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RC415MD (2 of 5) DDR2**

Size	Document Number	Rev
A3	Y4A	-1

Date: Tuesday, January 23, 2007 Sheet 7 of 49

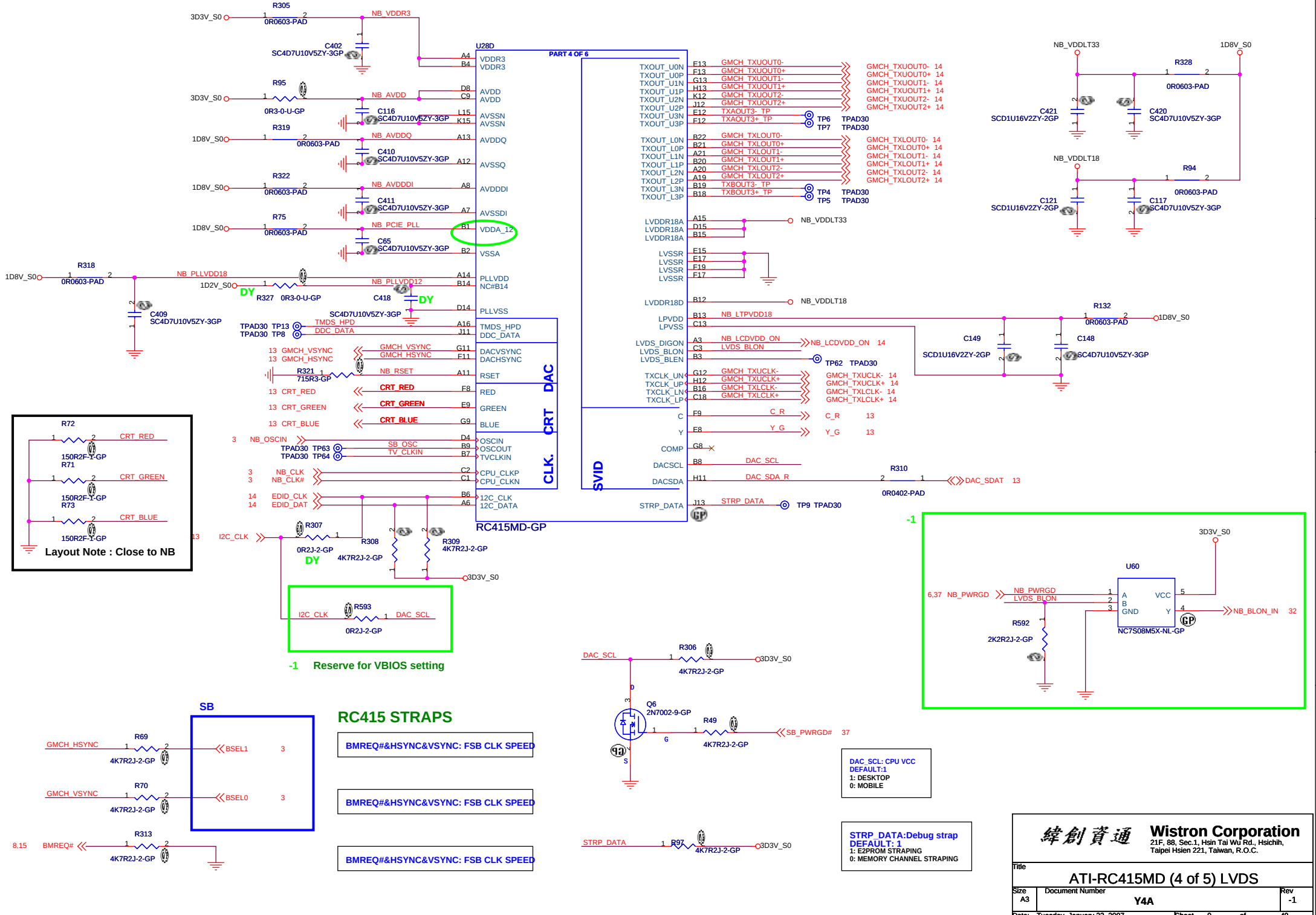


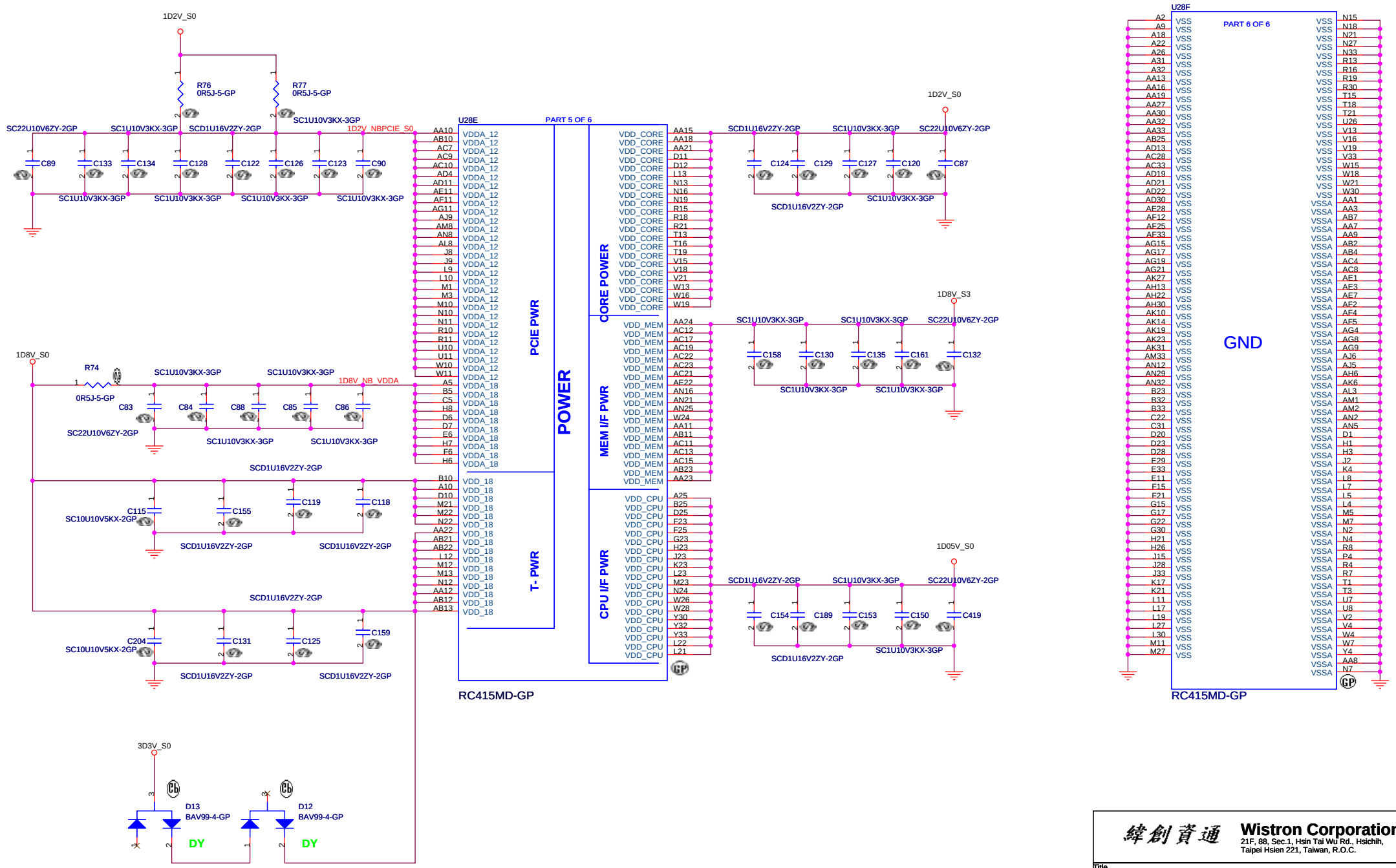
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RC415MD (3 of 5) PCIE

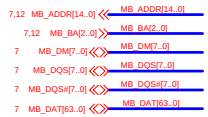
Size	Document Number	Rev
A3	Y4A	-1

Date: Tuesday, January 23, 2007 Sheet 8 of 49

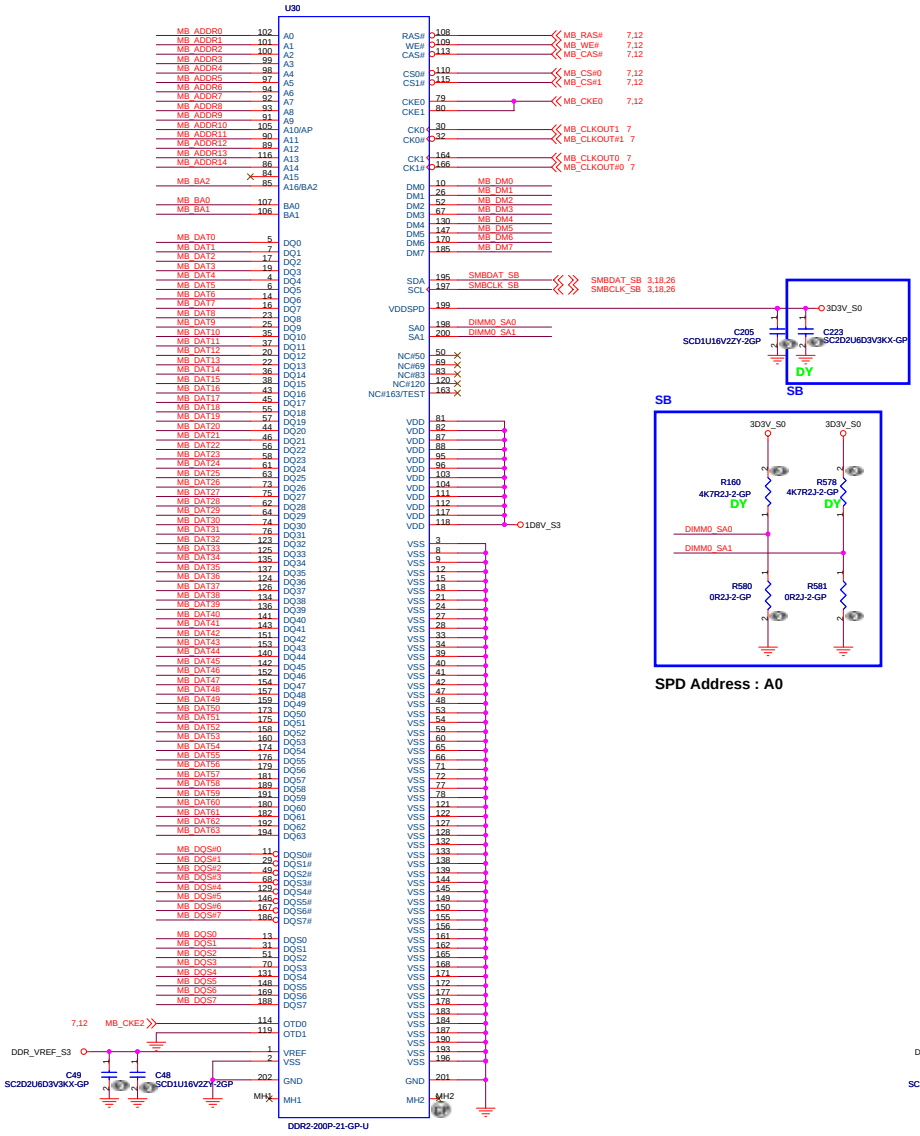

U28D
PART 4 OF 6
RC415MD-GP
R305 0R0603-PAD
C402 SC4D7U10V5ZY-3GP
R95 0R3-0-U-GP
C116 SC4D7U10V5ZY-3GP
R319 0R0603-PAD
C410 SC4D7U10V5ZY-3GP
R322 0R0603-PAD
C411 SC4D7U10V5ZY-3GP
R75 0R0603-PAD
C65 SC4D7U10V5ZY-3GP
R318 0R0603-PAD
C409 SC4D7U10V5ZY-3GP
R327 0R3-0-U-GP
C418 SC4D7U10V5ZY-3GP
R321 715R3-GP
R72 150R2F-1-GP
R71 150R2F-1-GP
R73 150R2F-1-GP
Layout Note : Close to NB
R307 0R2J-2-GP
R308 4K7R2J-2-GP
R309 4K7R2J-2-GP
R593 0R2J-2-GP
-1 Reserve for VBIOS setting
R328 0R0603-PAD
C421 SCD1U16V2ZY-2GP
C420 SC4D7U10V5ZY-3GP
R94 0R0603-PAD
C121 SCD1U16V2ZY-2GP
C117 SC4D7U10V5ZY-3GP
R132 0R0603-PAD
C149 SCD1U16V2ZY-2GP
C148 SC4D7U10V5ZY-3GP
R310 0R0402-PAD
U60 NC7S08M5X-NL-GP
R592 2K2R2J-2-GP
R306 4K7R2J-2-GP
Q6 2N7002-9-GP
R49 4K7R2J-2-GP
R97 4K7R2J-2-GP
SB
R69 4K7R2J-2-GP
R70 4K7R2J-2-GP
R313 4K7R2J-2-GP
RC415 STRAPS
BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
BMREQ#&HSYNC&VSYNC: FSB CLK SPEED
DAC_SCL: CPU VCC
DEFAULT:1
1: DESKTOP
0: MOBILE
STRP_DATA:Debug strap
DEFAULT: 1
1: E2PROM STRAPING
0: MEMORY CHANNEL STRAPING
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RC415MD (4 of 5) LVDS
Size A3
Document Number Y4A
Rev -1
Date: Tuesday, January 23, 2007
Sheet 9 of 49



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ATI-RC415MD (5 of 5) POWER	
Size: A3	Document Number: Y4A
Rev: -1	
Date: Tuesday, January 23, 2007	Sheet 10 of 49



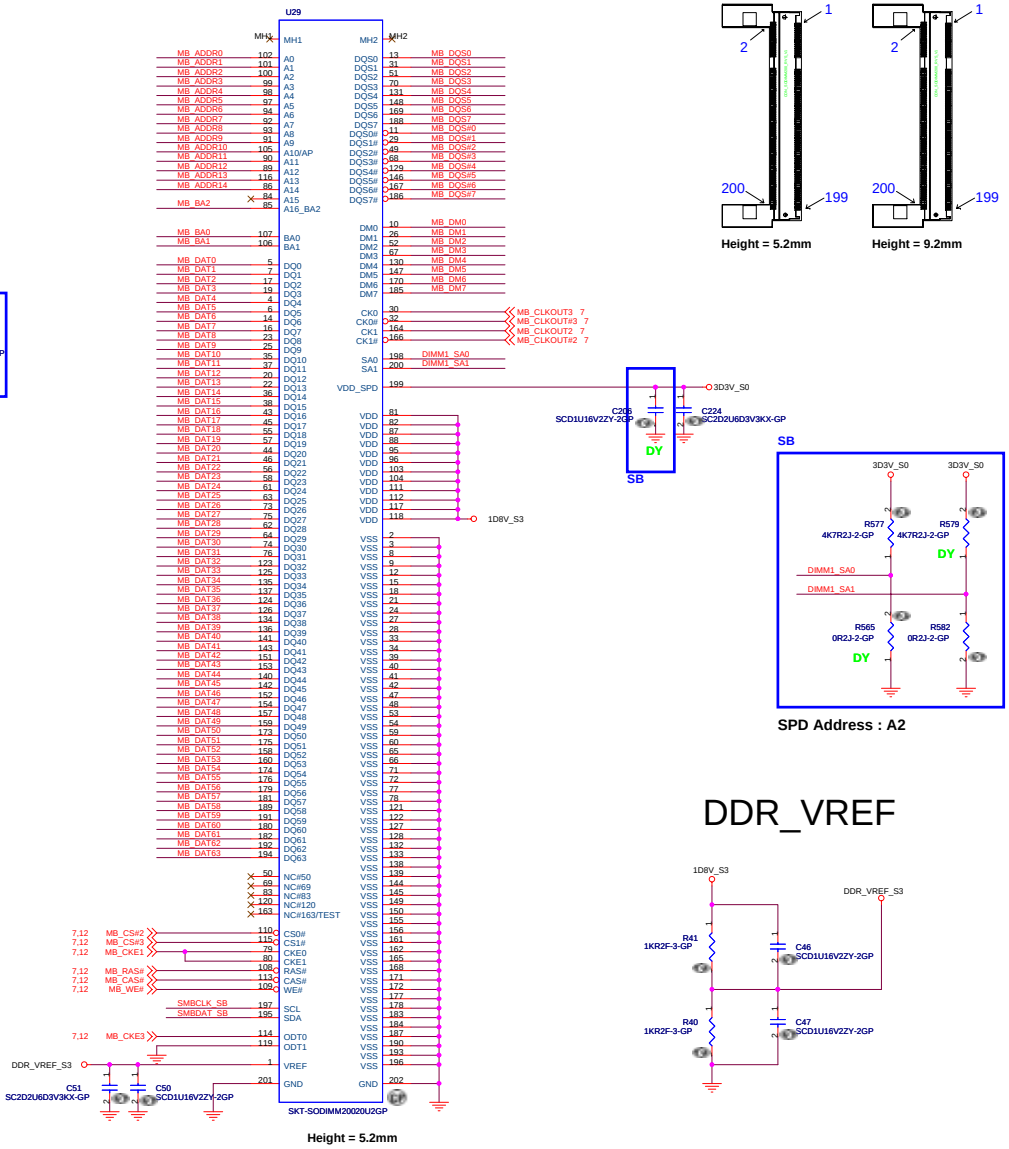
DIMM0



Height = 9.2mm

SPD Address : A0

DIMM1



Height = 5.2mm

Part Number change to 62.10017.A41

Height = 5.2mm

Height = 9.2mm

SPD Address : A2

DDR_VREF

LAYOUT: Locate close to DIMM

<Variant Name>

Wistron Corporation
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Title: DDR2-SOCKET

Size	Document Number	Rev
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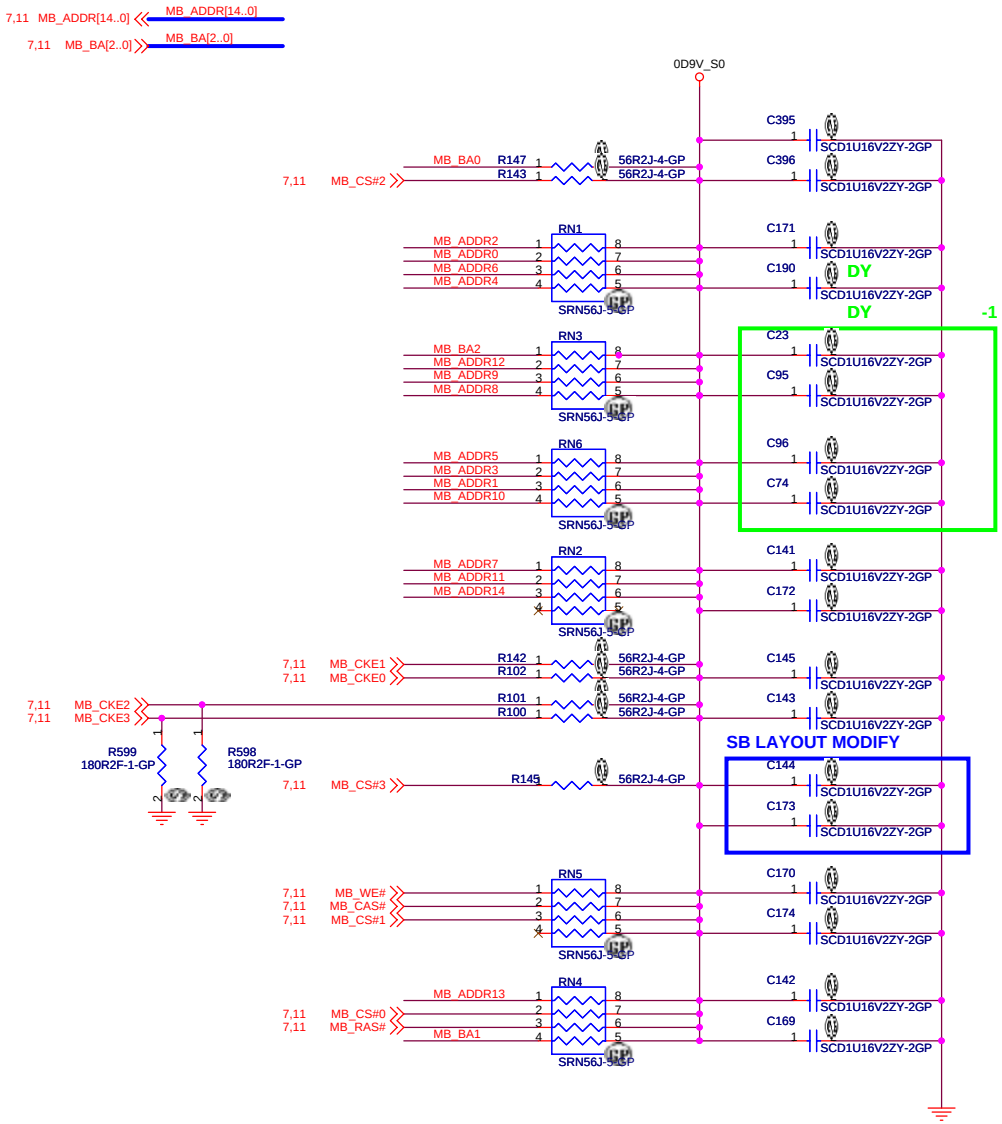
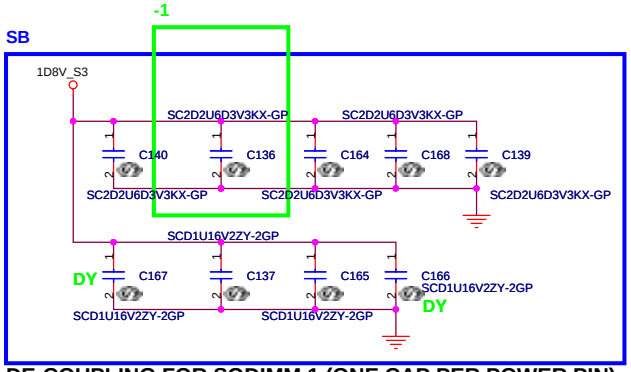
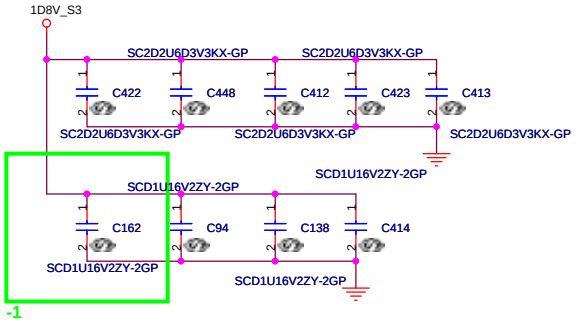
PARALLEL TERMINATION AND Decoupling Capacitor





DE-COUPLING FOR SODIMM 1 (ONE CAP PER POWER PIN)

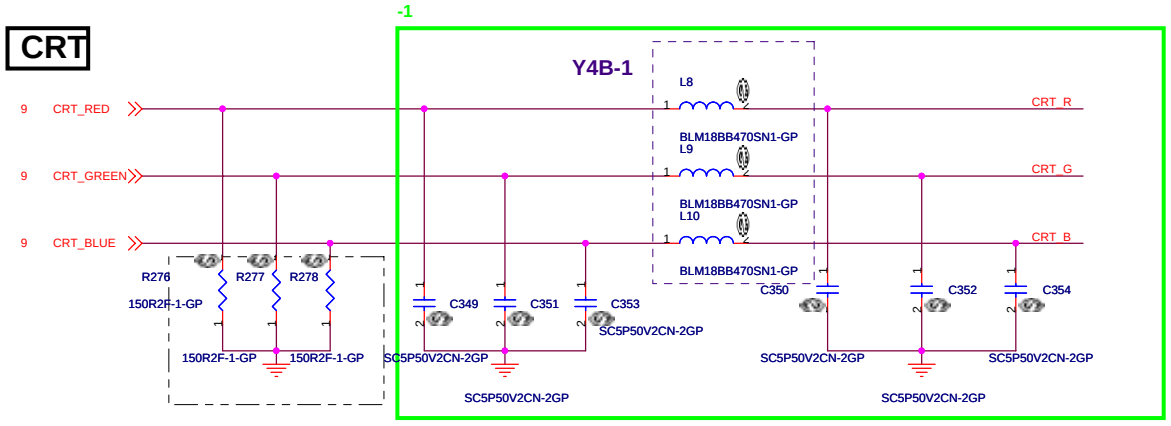


DE-COUPLING FOR SODIMM 1 (ONE CAP PER POWER PIN)

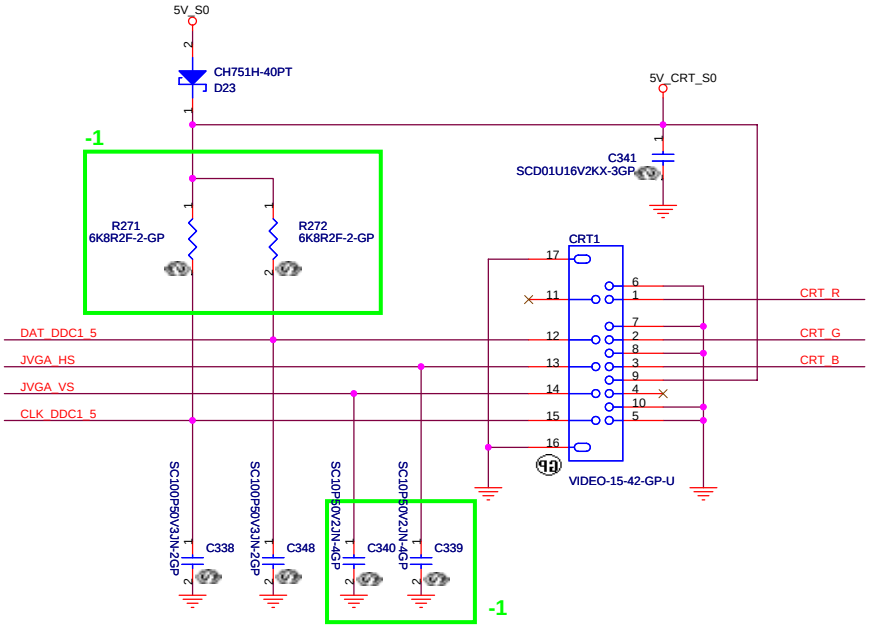
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

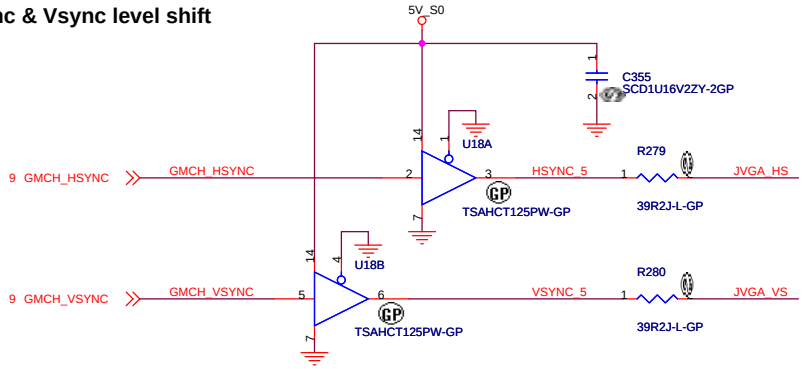
Title	DDR2-RESISTOR	
Size A3	Document Number Y4A	Rev -1
Date: Tuesday, January 23, 2007	Sheet 12 of 49	

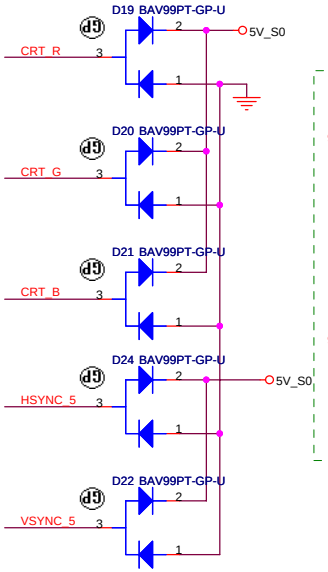


LAYOUT NOTE :
CLOSE TO CRT CONNECTOR, THE TRACE IMPEDANCE BETWEEN NB AND 150OHM RESISTOR SHOULD BE 37.5OHM+/-15%, BETWEEN TWO 150OHM RESISTORS SHOULD BE 50OHM, BETWEEN 150OHM RESISTOR AND CONNECTOR SHOULD BE 75OHM+/-15%



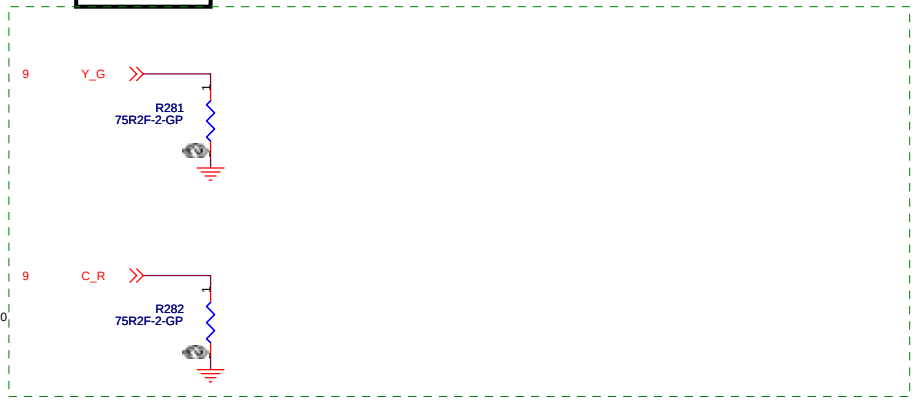
Hsync & Vsync level shift



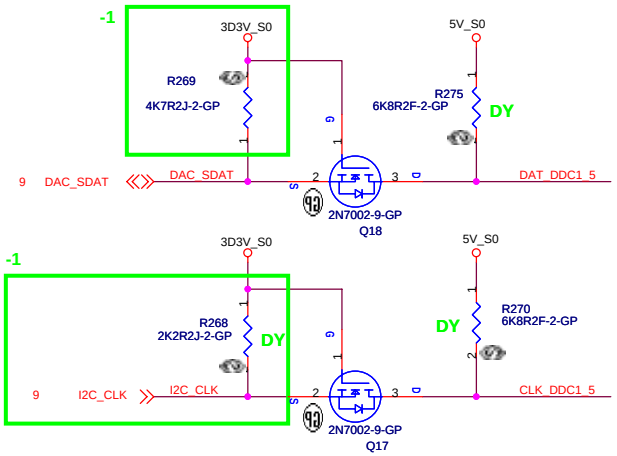


S-Video

Y4B delete component for ME



DDC_CLK & DATA level shift



R911-R913 EITHER CLOSE TO NB OR TV CONNECTOR, THE TRACE IMPEDANCE BETWEEN NB AND 75OHM RESISTOR SHOULD BE 37.5OHM+/-15%, THE TRACE IMPEDANCE BETWEEN 75OHM RESISTOR AND CONNECTOR SHOULD BE 75OHM+/-15%

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT/TV Connector***

Size	Document Number	Rev
A3	Y4A	-1

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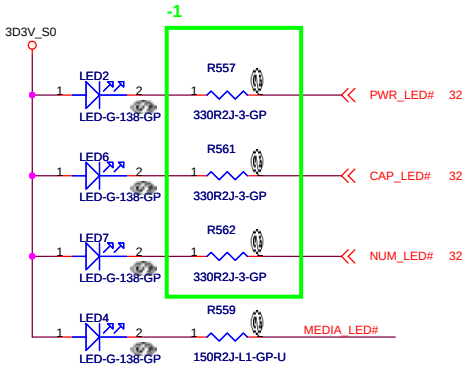
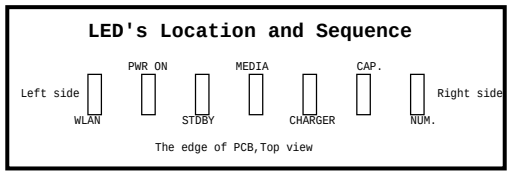
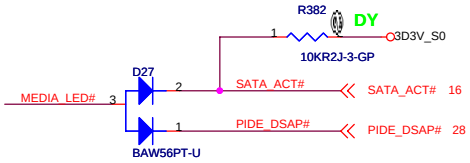
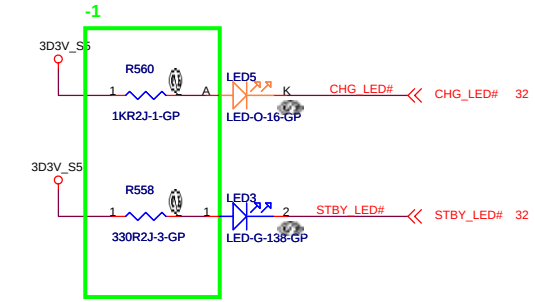
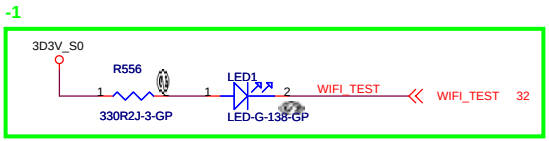
LED



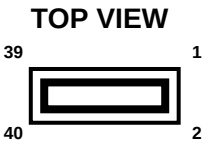


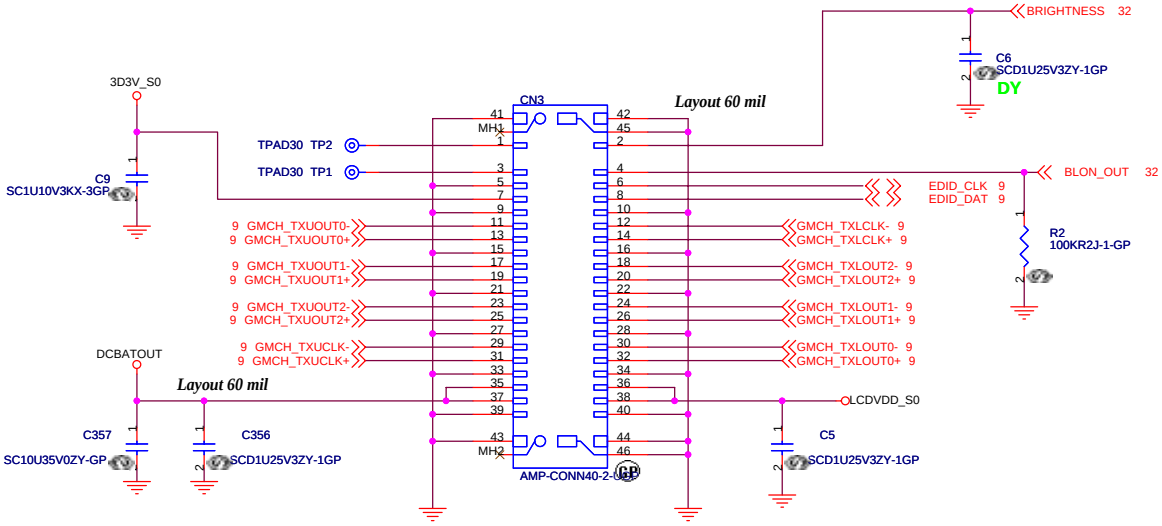




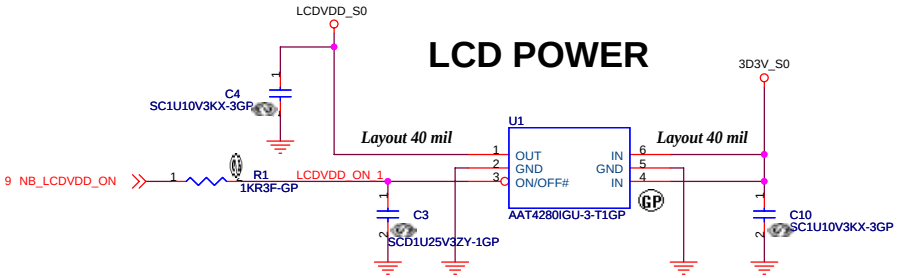


LCD/INVERTER/CCD CONN





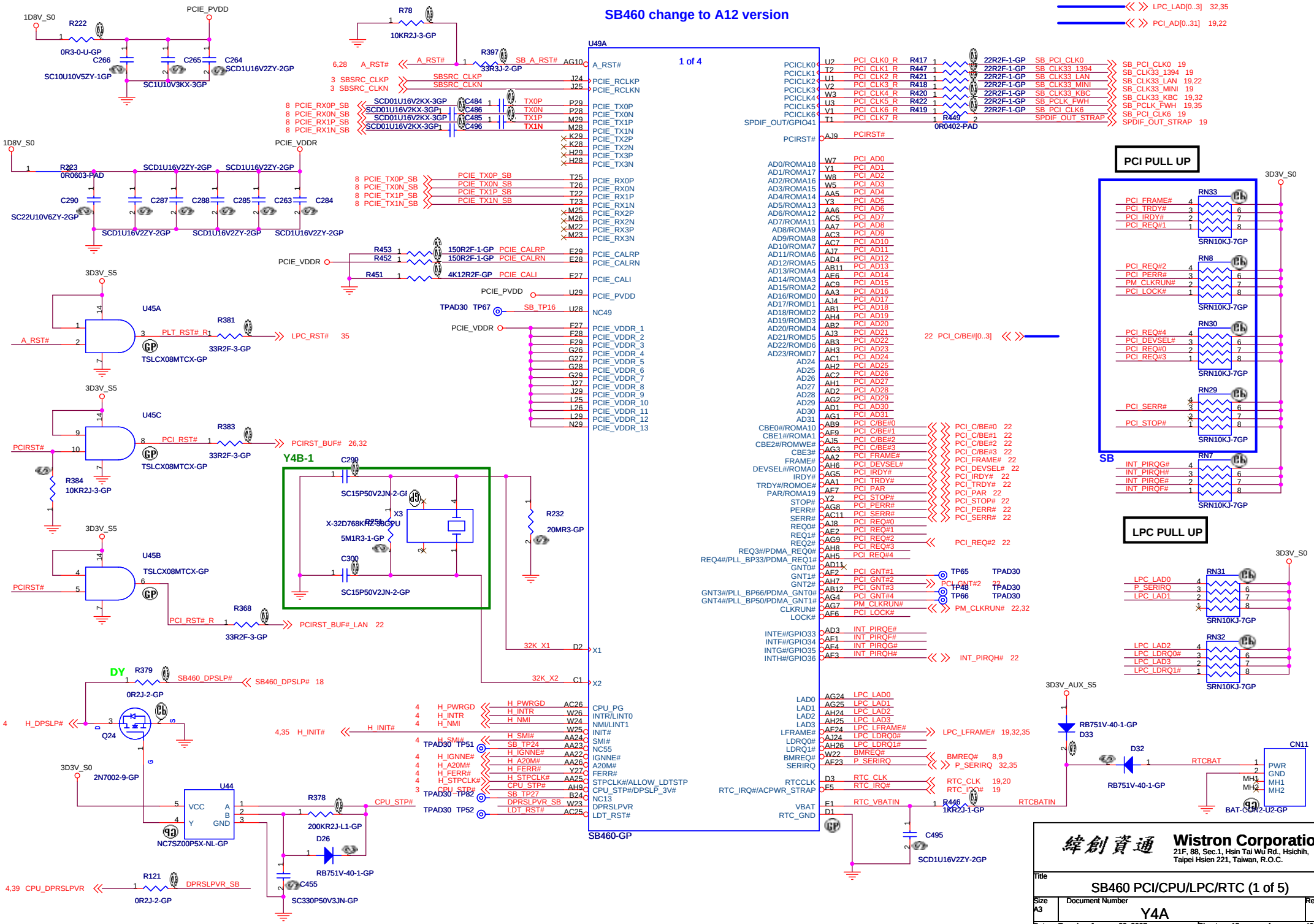
LCD POWER

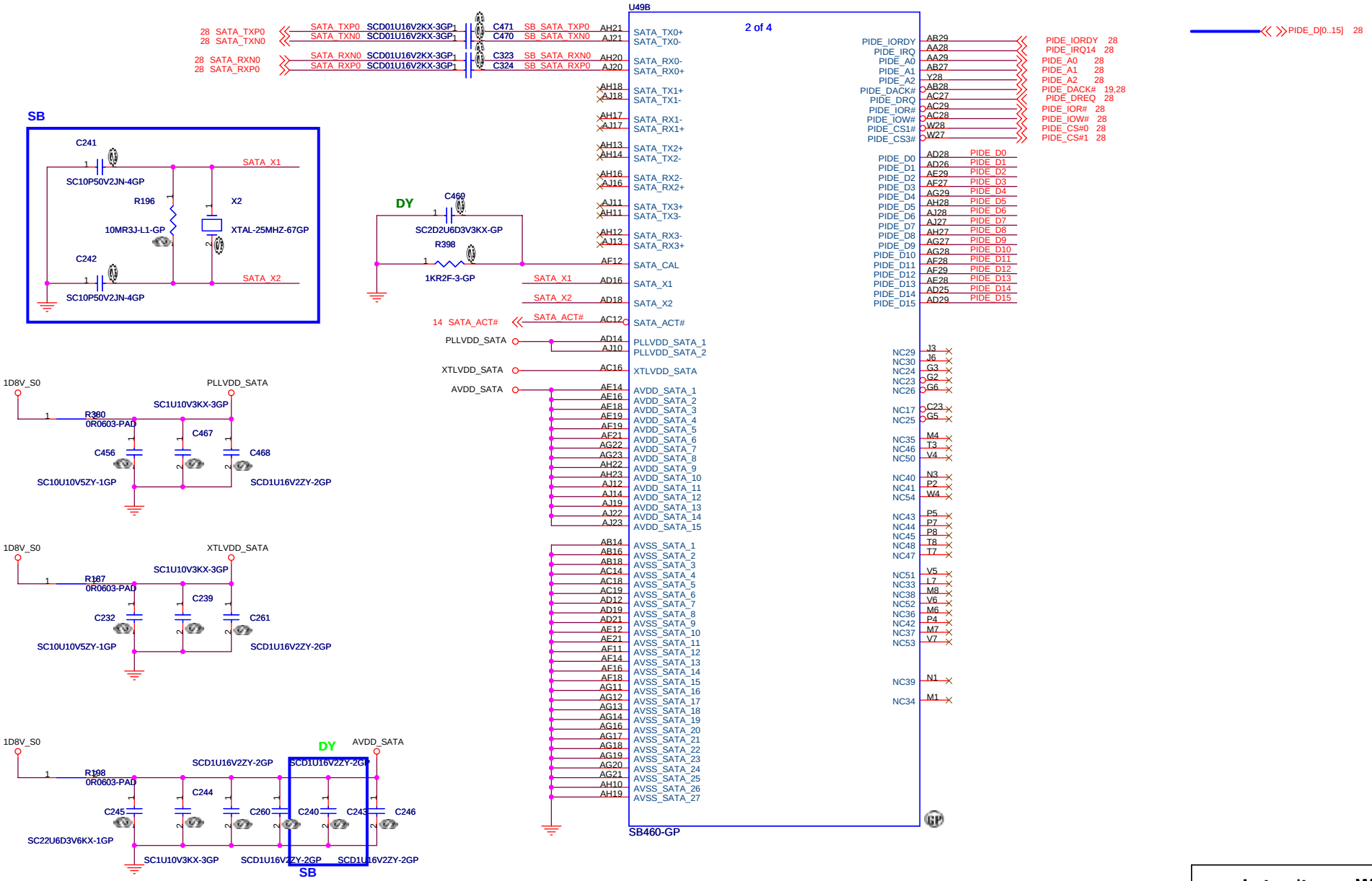


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INVERTER / LCD	
Size A3	Document Number Y4A	Rev -1
Date: Tuesday, January 23, 2007	Sheet 14 of 49	

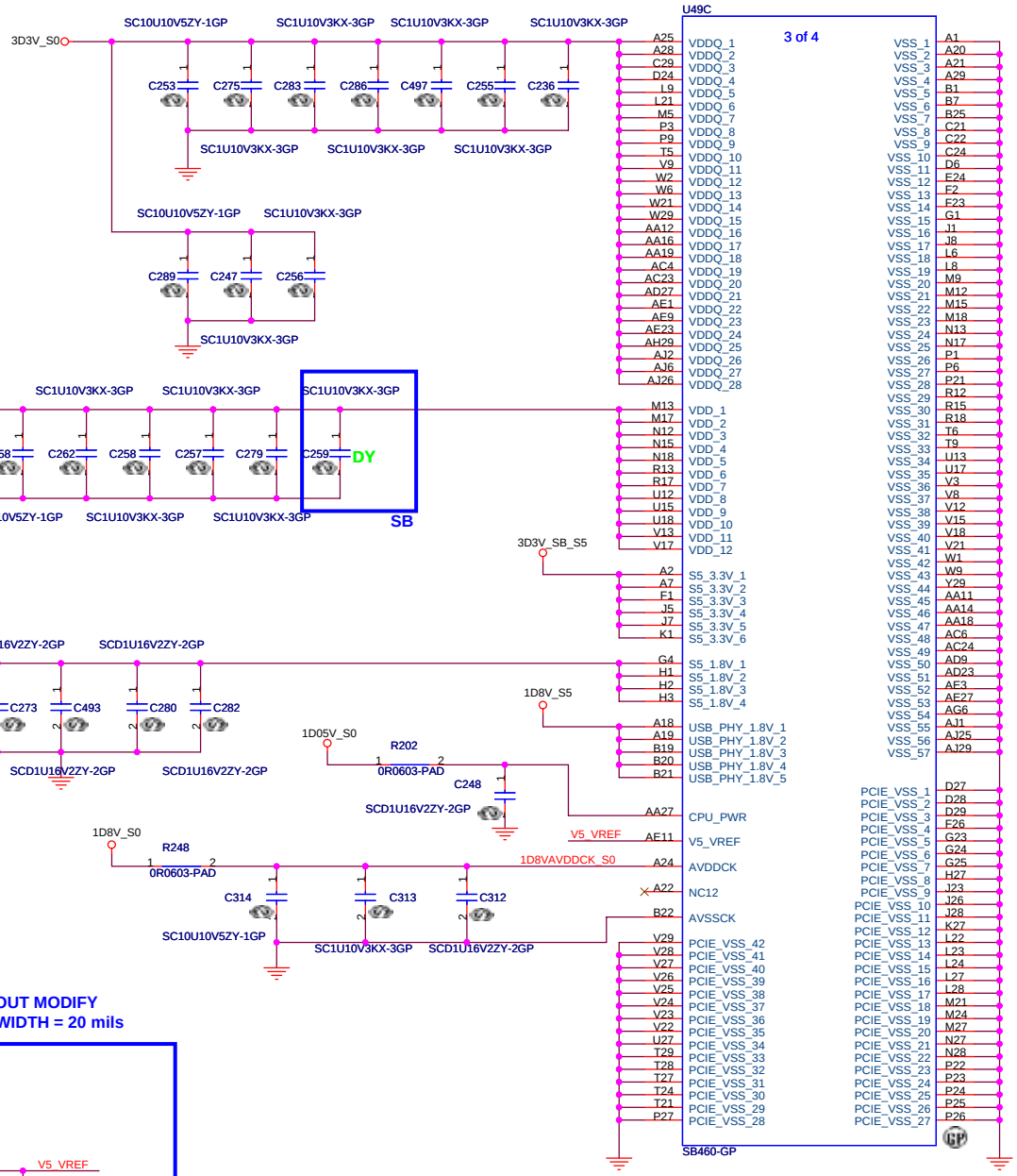
SB460 change to A12 version





Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB460 ACPI/GPIO/SATA/IDE (2 of 5)
Size A3	Document Number Y4A
Rev	-1
Date: Tuesday, January 23, 2007	Sheet 16 of 49

ATI FAE Note :
Please refer to ATI reference design to change the high frequency decoupling caps on VDDQ and VDD from 0.1uF to 1uF

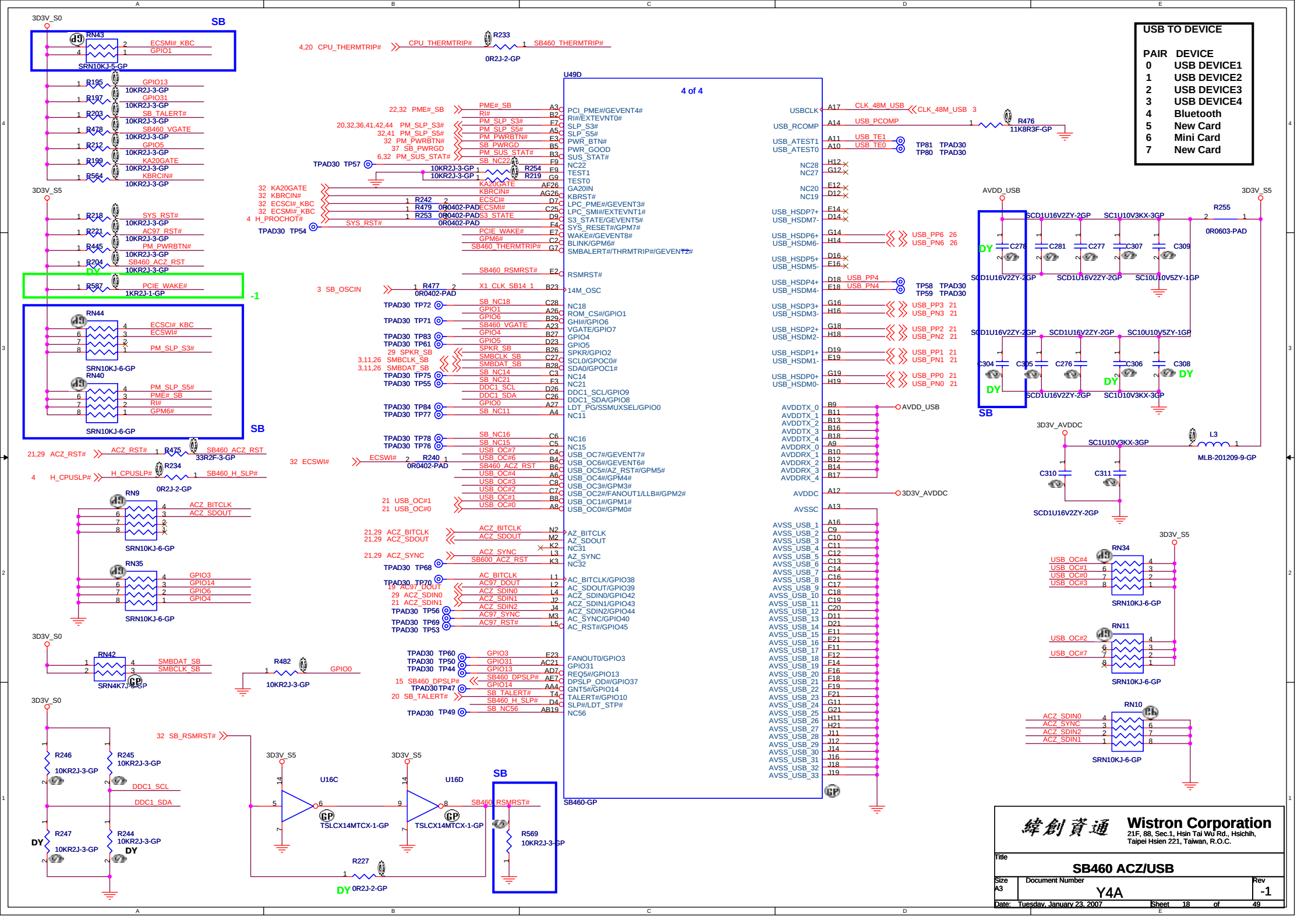


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

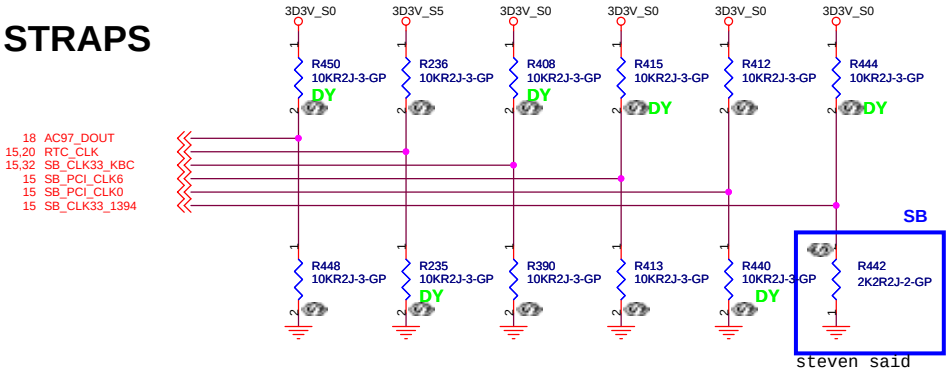
Title: **SB460 POWER/DECOUPLING**

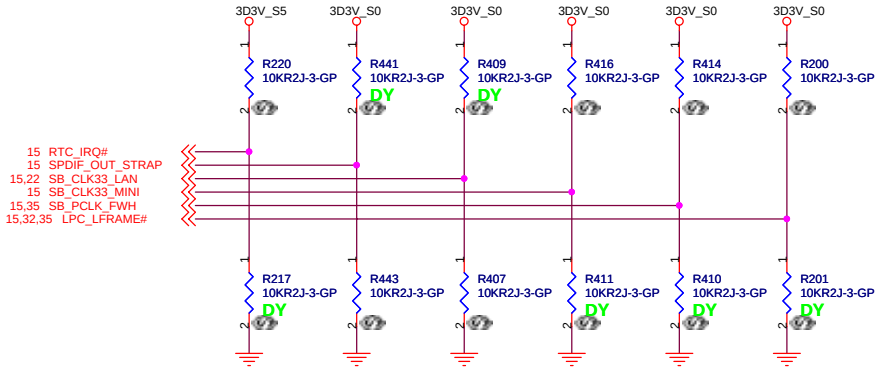
Size	Document Number	Rev
A3	Y4A	-1

Date: Tuesday, January 23, 2007 Sheet 17 of 49


USB TO DEVICE
PAIR DEVICE
0 USB DEVICE1
1 USB DEVICE2
2 USB DEVICE3
3 USB DEVICE4
4 Bluetooth
5 New Card
6 Mini Card
7 New Card
U49D
4 of 4
SB460-GP
SB
DY
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB460 ACZ/USB
Size A3
Document Number
Y4A
Rev -1
Date: Tuesday, January 23, 2007
Sheet 18 of 49

REQUIRED STRAPS



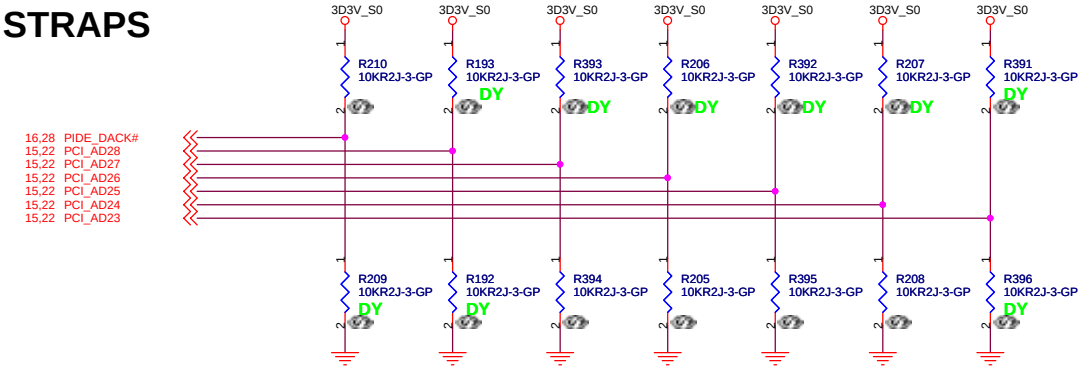


PCI_CLK0 NONE
PCI_CLK1 IEEE1394
PCI_CLK2 LAN
PCI_CLK3 MINI
PCI_CLK4 KBC
PCI_CLK5 FWH
PCI_CLK6 NONE
PCI_CLK7 SPDIFOUT

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	SB600 PCI_CLK0 PCI_CLK1	SB460 PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM DEFAULT L, H = LPC II ROM L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT		

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

DEBUG STRAPS



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB460 ONLY SB600 ONLY

SB600 ONLY

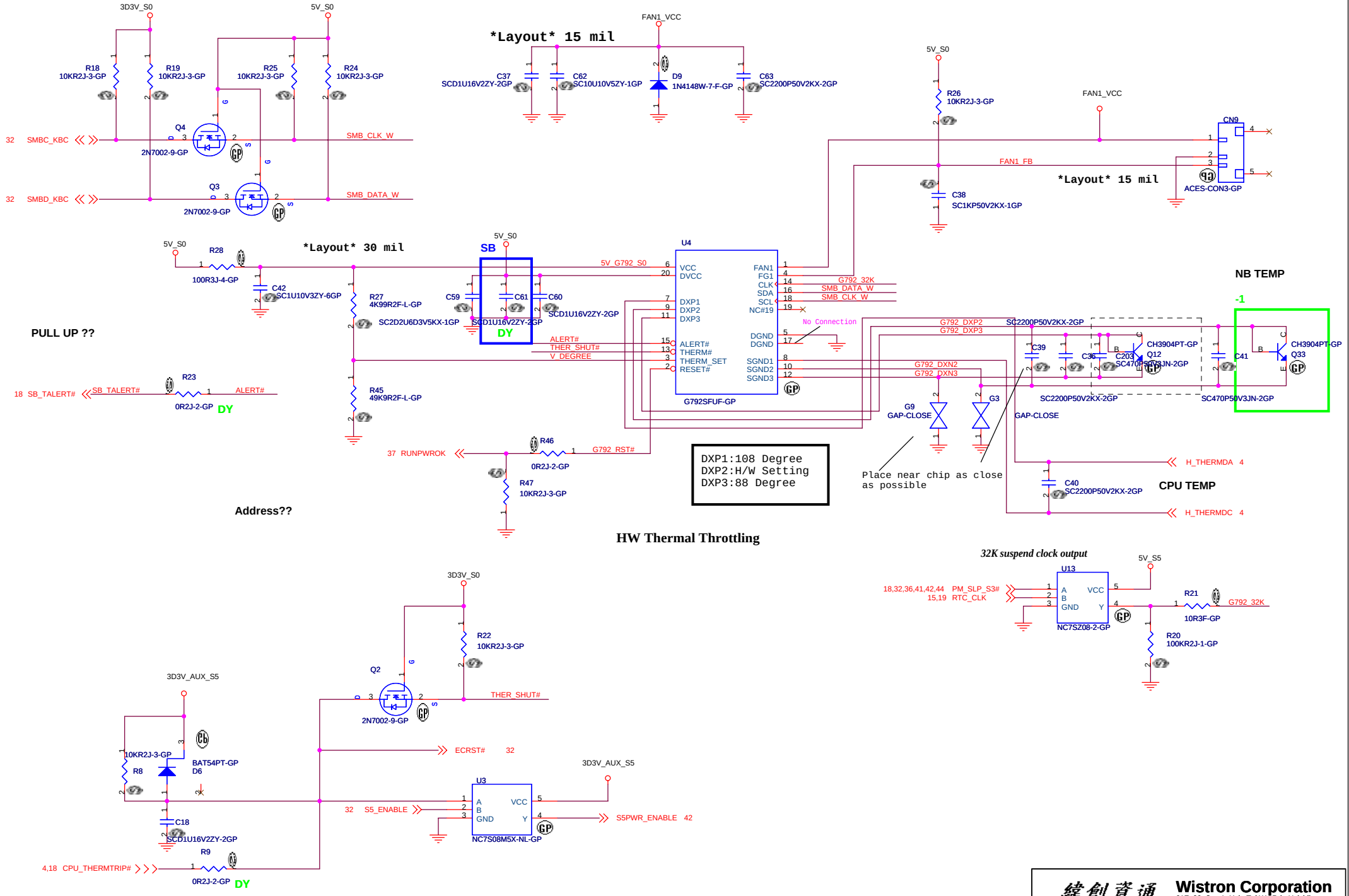
NOTE: FOR SB460, PCI_AD23 IS RESERVED

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SB460 STRAPPING PIN**

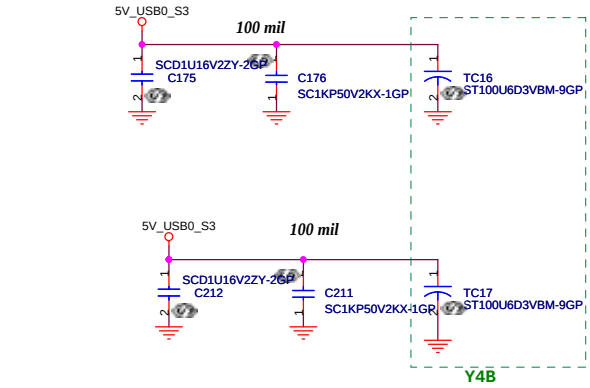
Size	Document Number	Rev
A3	Y4A	-1

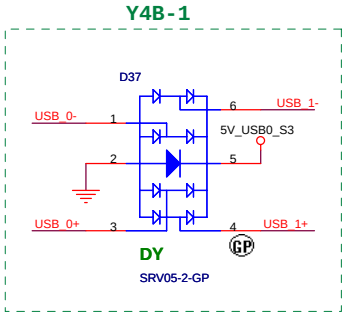
Date: Tuesday, January 23, 2007 Sheet 19 of 49

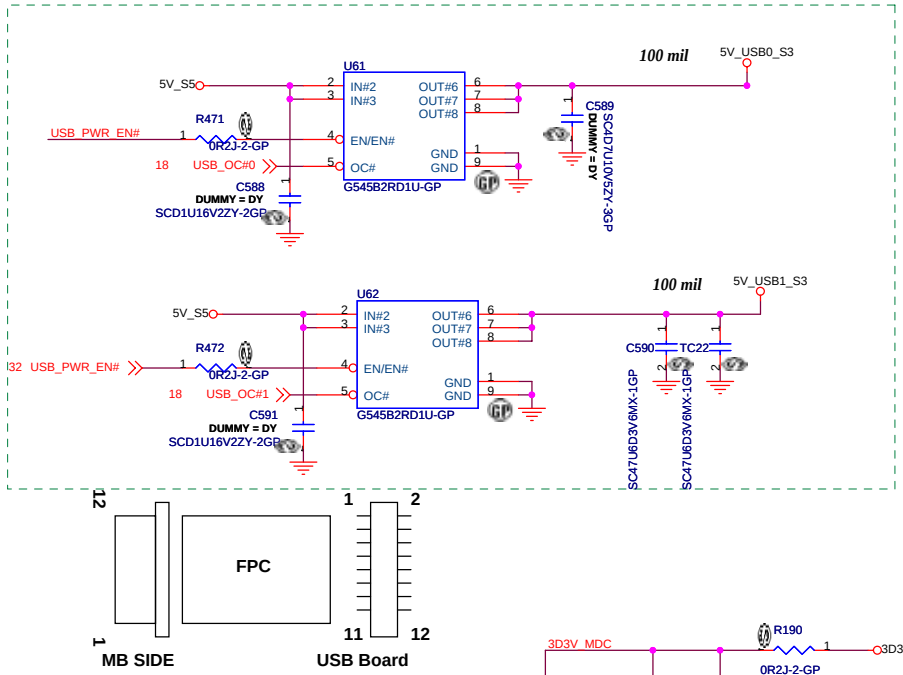


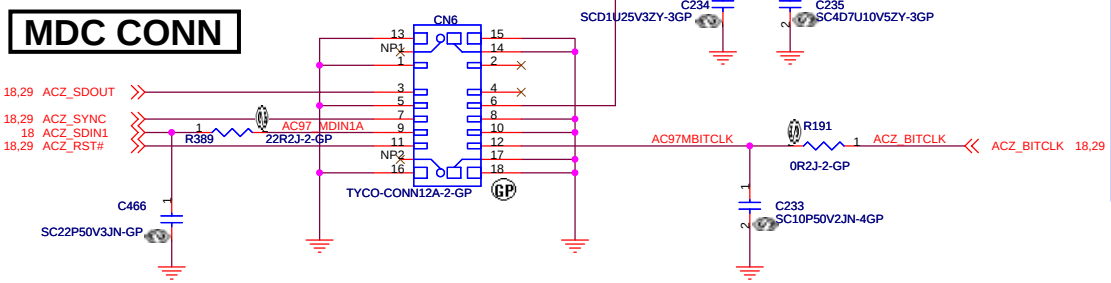
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***G792***	
Size A3	Document Number Y4A	Rev -1
Date: Tuesday, January 23, 2007	Sheet 20 of 49	

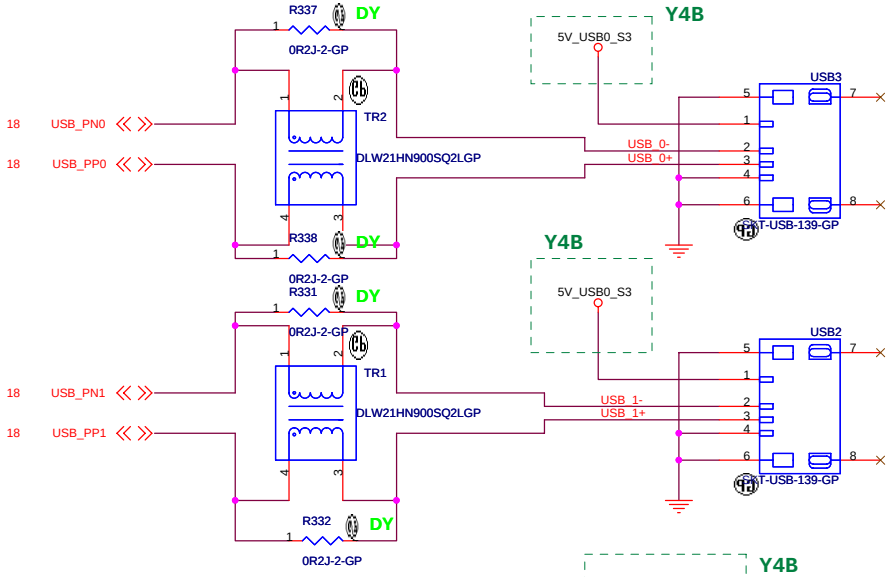
USB PORT

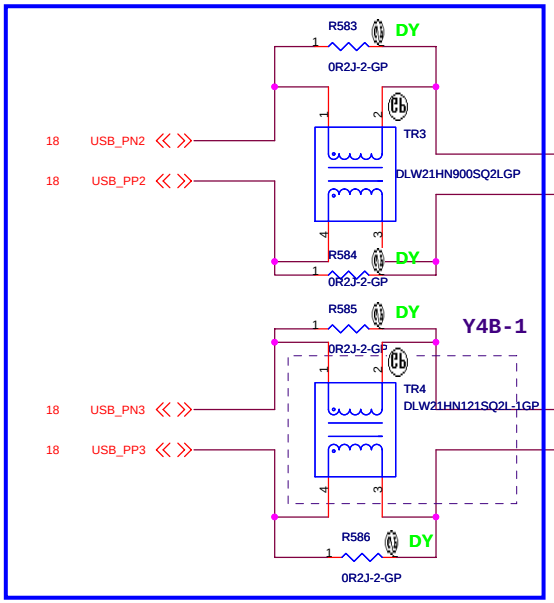


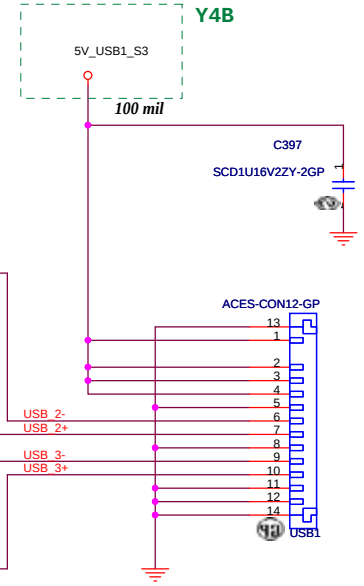




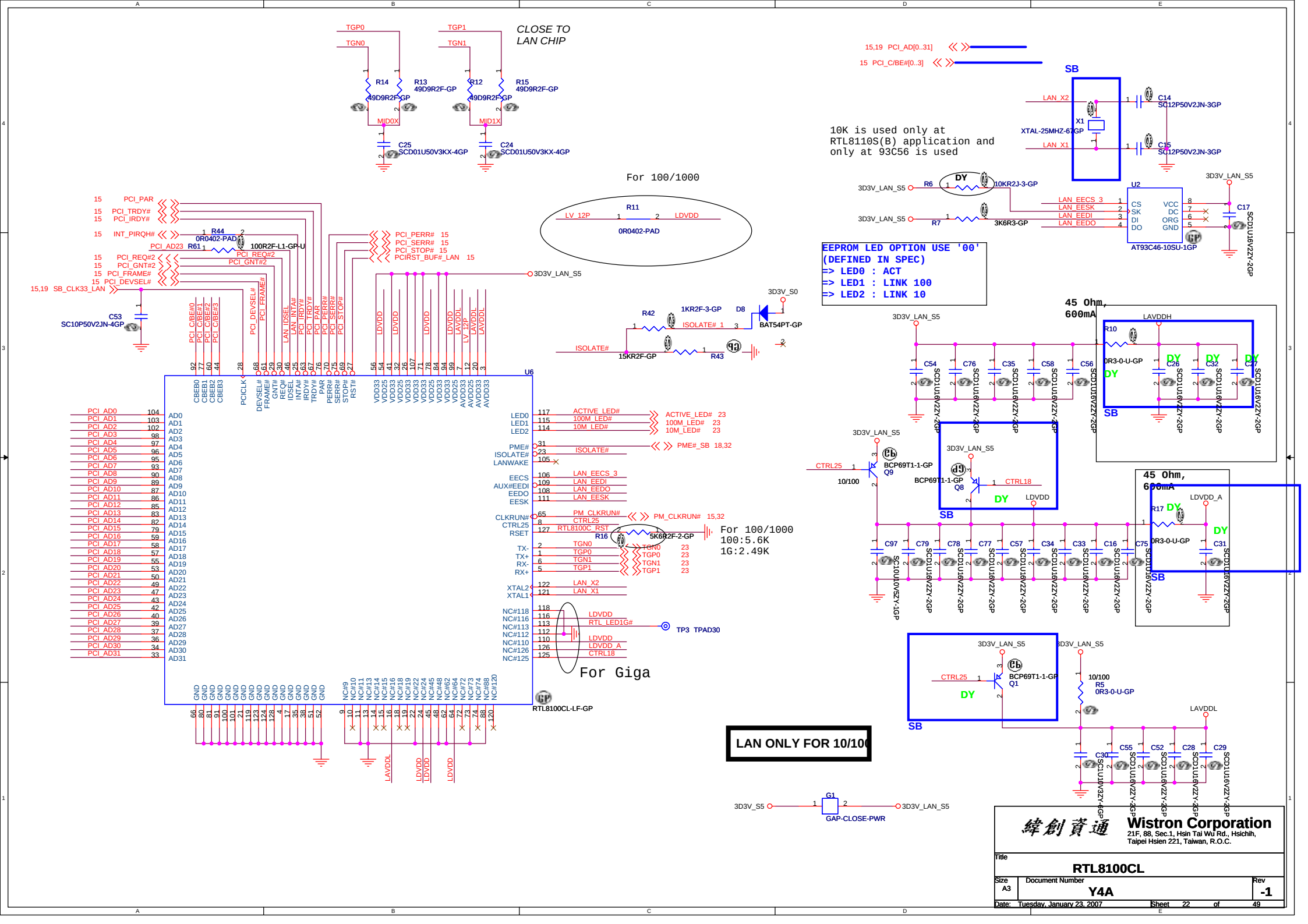








緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB/MDC/BT and TV TURNER I/F		
Size: A3	Document Number: Y4A	Rev: -1
Date: Tuesday, January 23, 2007	Sheet 21 of 49	


CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
R14 49D9R2F-GP
R13 49D9R2F-GP
R12 49D9R2F-GP
R15 49D9R2F-GP
MID0X
MID1X
C25 SCD01U50V3KX-4GP
C24 SCD01U50V3KX-4GP
For 100/1000
R11 0R0402-PAD
LV_12P
LDVDD
15,19 PCI_AD[0..31]
15 PCI_C/BE#[0..3]
SB
LAN_X2
LAN_X1
X1 XTAL-25MHZ-6PGP
C14 SC12P50V2JN-3GP
C15 SC12P50V2JN-3GP
10K is used only at RTL8110S(B) application and only at 93C56 is used
3D3V_LAN_S5
R6 10KR2J-3-GP
R7 3K6R3-GP
DY
U2
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
CS SK DI DO VCC DC ORG GND
AT93C46-10SU-1GP
C17 SCD1U16V2ZY-2GP
EEPROM LED OPTION USE '00' (DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK 100
=> LED2 : LINK 10
15 PCI_PAR
15 PCI_TRDY#
15 PCI_IRDY#
15 INT_PIRQH#
PCI_AD23
R61
R44 0R0402-PAD
100R2F-L1-GP-U
15 PCI_REQ#2
15 PCI_GNT#2
15 PCI_FRAME#
15 PCI_DEVSEL#
15,19 SB_CLK33_LAN
C53 SC10P50V2JN-4GP
PCI_REQ#2
PCI_GNT#2
PCI_PERR# 15
PCI_SERR# 15
PCI_STOP# 15
PCIRST_BUF#_LAN 15
3D3V_LAN_S5
3D3V_S0
R42 1KR2F-3-GP
D8 BAT54PT-GP
ISOLATE#_1
ISOLATE#
15KR2F-GP
R43
U6
PCI_AD0 104
PCI_AD1 103
PCI_AD2 102
PCI_AD3 98
PCI_AD4 97
PCI_AD5 96
PCI_AD6 95
PCI_AD7 93
PCI_AD8 90
PCI_AD9 89
PCI_AD10 87
PCI_AD11 86
PCI_AD12 85
PCI_AD13 83
PCI_AD14 82
PCI_AD15 79
PCI_AD16 59
PCI_AD17 58
PCI_AD18 57
PCI_AD19 55
PCI_AD20 53
PCI_AD21 50
PCI_AD22 49
PCI_AD23 47
PCI_AD24 43
PCI_AD25 42
PCI_AD26 40
PCI_AD27 39
PCI_AD28 37
PCI_AD29 36
PCI_AD30 34
PCI_AD31 33
LED0 117 ACTIVE_LED# ACTIVE_LED# 23
LED1 115 100M_LED# 100M_LED# 23
LED2 114 10M_LED# 10M_LED# 23
PME# 31 PME#_SB 18,32
ISOLATE# 23 ISOLATE#
LANWAKE 105
EECS 106 LAN_EECS_3
AUX#EEDI 109 LAN_EEDI
EEDO 108 LAN_EEDO
EESK 111 LAN_EESK
CLKRUN# 65 PM_CLKRUN# PM_CLKRUN# 15,32
CTRL25 8
RSET 127 RTL8100C_RST
R16 5K6R2F-2-GP
For 100/1000
100:5.6K
1G:2.49K
TX- 2 TGN0 TGN0 23
TX+ 1 TGP0 TGP0 23
RX- 6 TGN1 TGN1 23
RX+ 5 TGP1 TGP1 23
XTAL2 122 LAN_X2
XTAL1 121 LAN_X1
NC#118 118
NC#116 116 LDVDD
NC#113 113 RTL_LED1G#
NC#112 112
NC#110 110 LDVDD
NC#126 126 LDVDD_A
NC#125 125 CTRL18
TP3 TPAD30
For Giga
RTL8100CL-LF-GP
45 Ohm, 600mA
LAVDDH
R10 0R3-0-U-GP
C54 C76 C35 C58 C56 C26 C32 C27 SCD1U16V2ZY-2GP
3D3V_LAN_S5
CTRL25
10/100
BCP69T1-1-GP Q9
BCP69T1-1-GP Q8
CTRL18
LDVDD
C97 C79 C78 C77 C57 C34 C33 C16 C75 SCD1U16V2ZY-2GP
SC10U10V5ZY-1GP
LDVDD_A
R17 0R3-0-U-GP
C31 SCD1U16V2ZY-2GP
BCP69T1-1-GP Q1
R5 0R3-0-U-GP
LAVDDL
C30 SC10U10V3ZY-4GP
C55 C52 C28 C29 SCD1U16V2ZY-2GP
LAN ONLY FOR 10/10
3D3V_S5
G1 GAP-CLOSE-PWR
3D3V_LAN_S5
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8100CL
Size A3
Document Number Y4A
Rev -1
Date: Tuesday, January 23, 2007
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LAN Connector

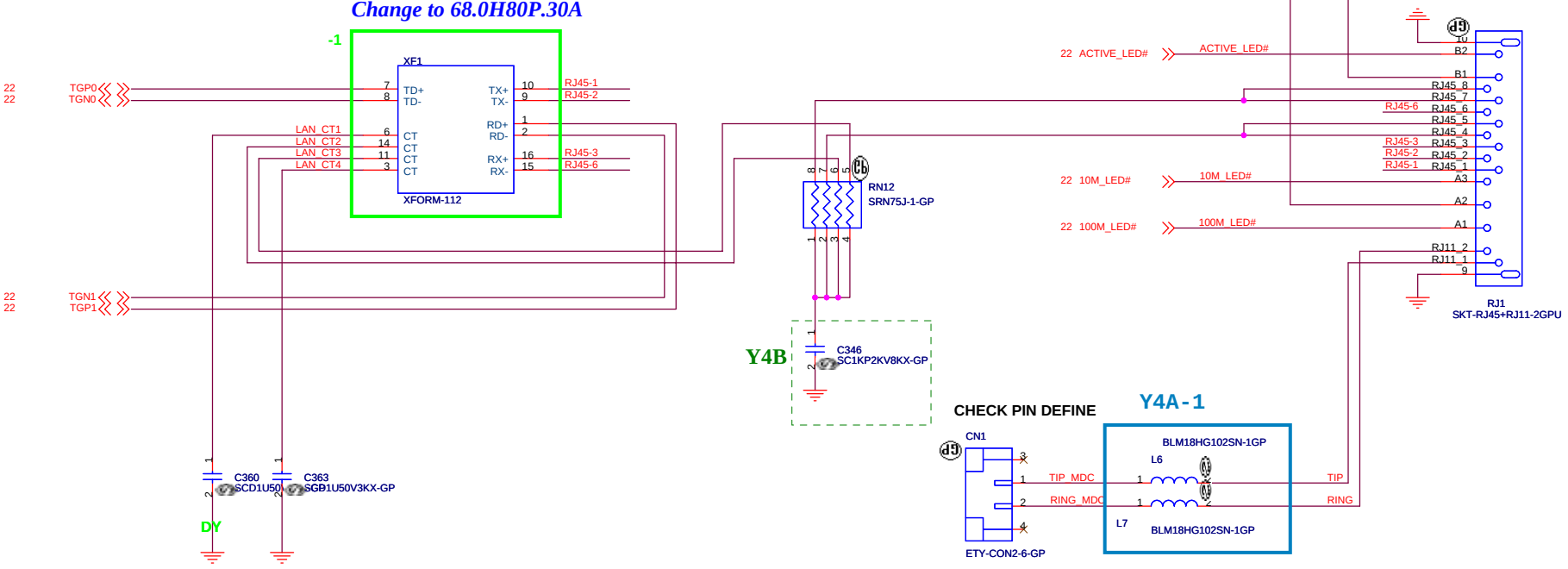
10/100

Green - 100M
Yellow - Active
Orange - 10M

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,6mil separation.
6.36mil between pairs and any other signal trace.
7.12 mil between other paires.
8.Must not cross ground moat .

Change to 68.0H80P.30A

-1



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
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Date: Tuesday, January 23, 2007 Sheet 23 of 49

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**R5C832_PCI(1/2)**
Size: A3	Document Number: **Y4A**
Rev: **-1**	
Date: Tuesday, January 23, 2007	Sheet 24 of 49

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***R5C832_1394_7IN1(2/2)***	
Size: A3	Document Number: **Y4A**	Rev: **-1**
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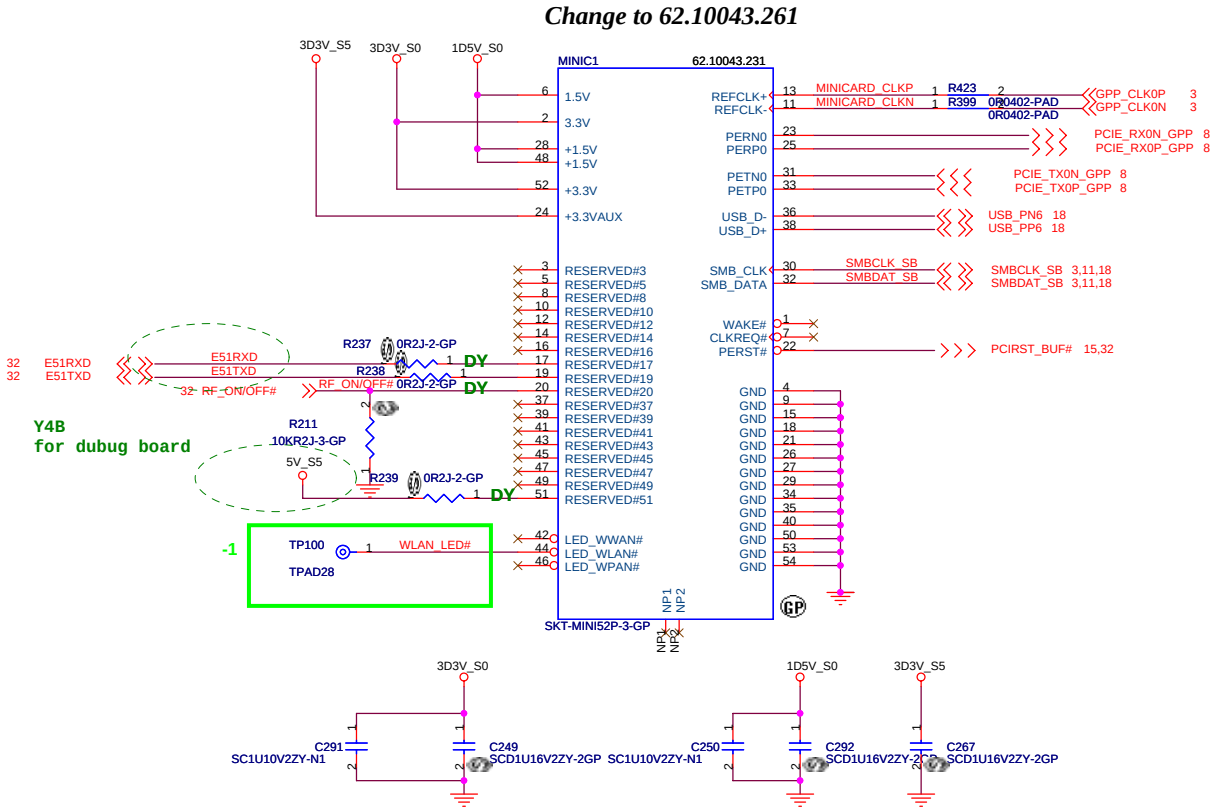
Mini Card Connector



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	MINI-PCI / MINI CARD		
Size A3	Document Number Y4A		Rev -1
Date: Tuesday, January 23, 2007		Sheet 26 of 49	

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***NEWCARD Connector***

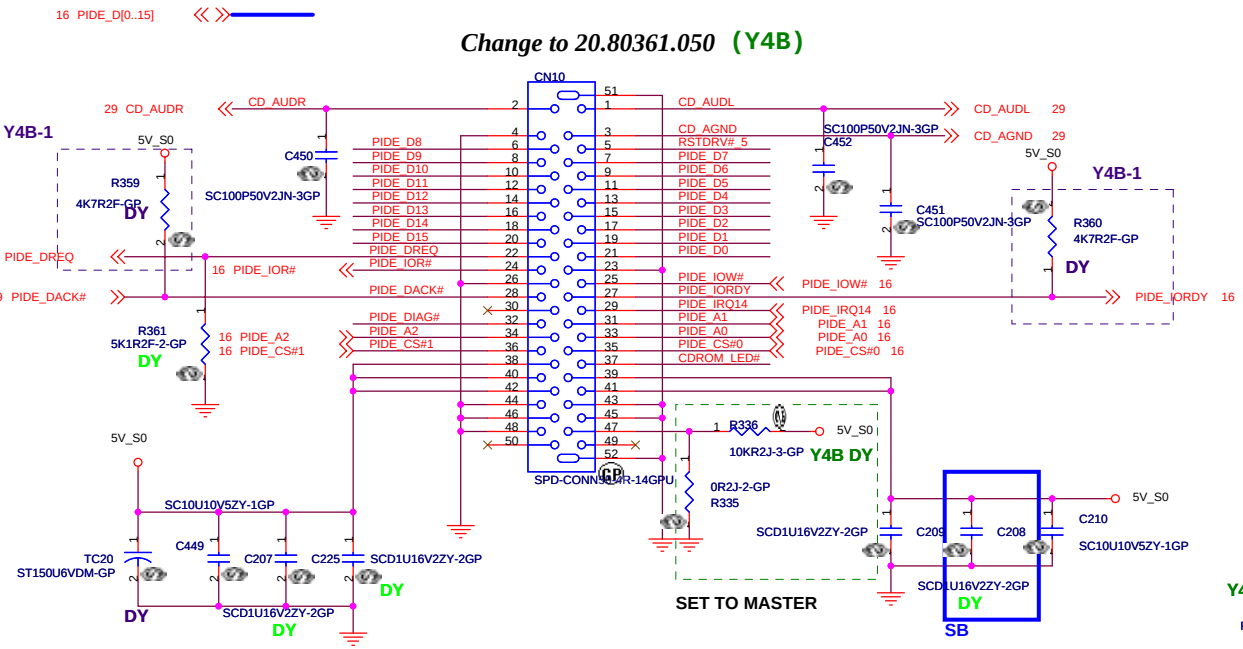
Size	Document Number	Rev
A3	Y4A	-1

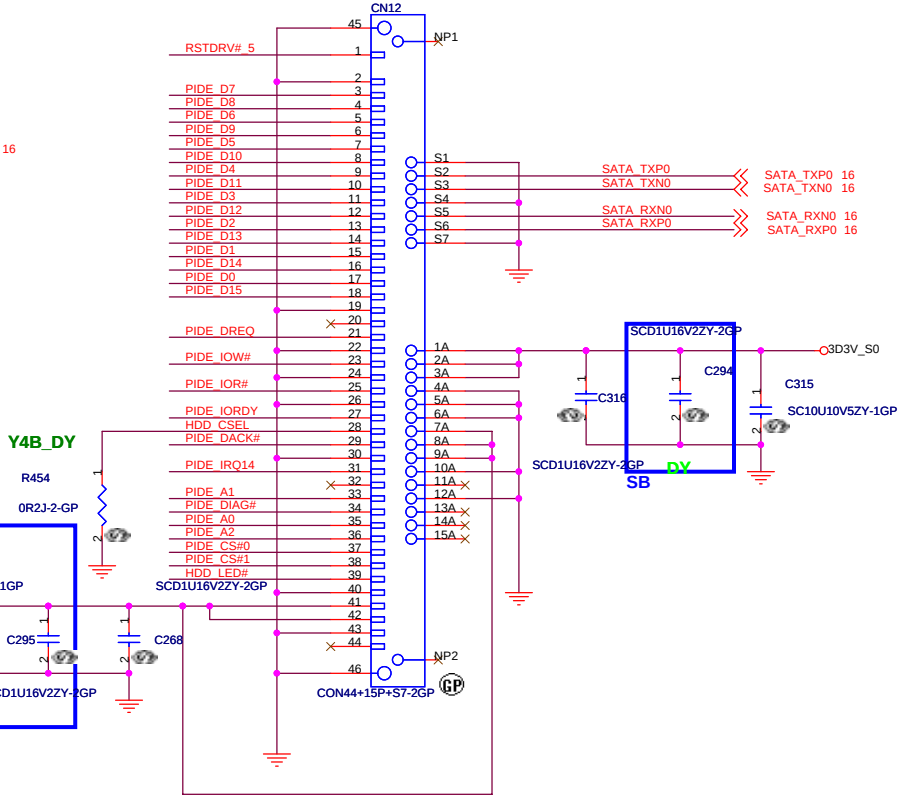
Date: Tuesday, January 23, 2007 Sheet 27 of 49

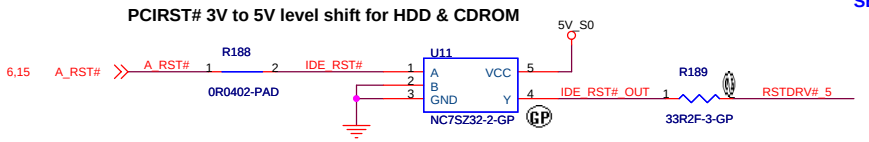
ODD Connector

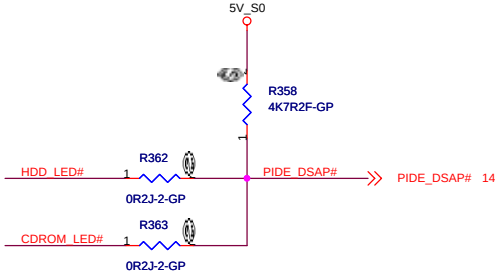
HD Connector (IDE / SATA)

Change to 20.80361.050 (Y4B)





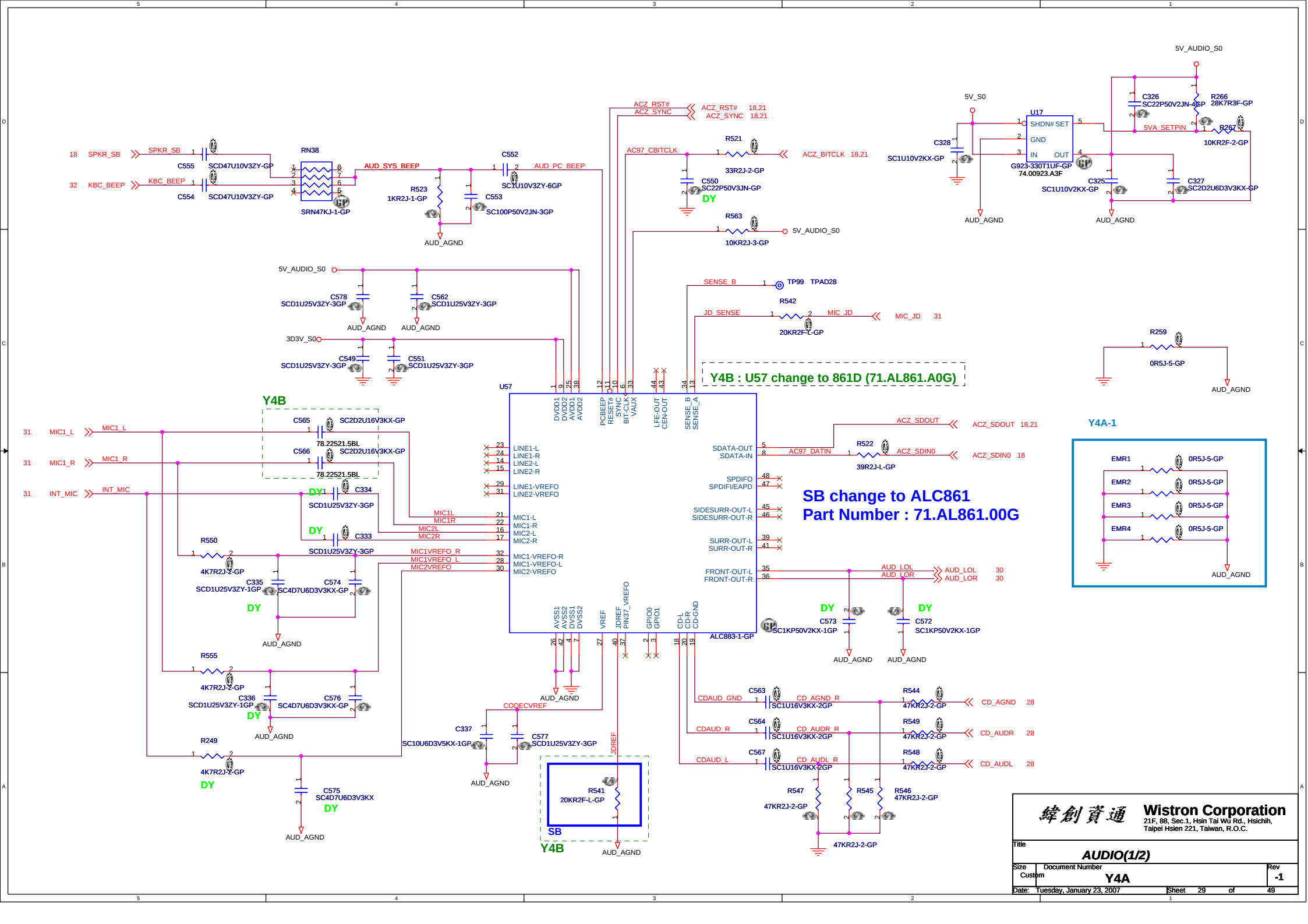




SATA : 20.F0885.001(Y4B)
PATA : 20.F0834.001(Y4A)

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD/CDROM CONN***	
Size A3	Document Number **Y4A**	Rev -1
Date: Tuesday, January 23, 2007	Sheet 28 of 49	


Y4B : U57 change to 861D (71.AL861.A0G)
SB change to ALC861
Part Number : 71.AL861.00G
U57
ALC883-1-GP
Y4B
Y4A-1
SB
DY
5V_AUDIO_S0
3D3V_S0
AUD_AGND
SPKR_SB
KBC_BEEP
AUD_SYS_BEEP
AUD_PC_BEEP
ACZ_RST#
ACZ_SYNC
ACZ_BITCLK
AC97_CBITCLK
SENSE_B
JD_SENSE
MIC_JD
MIC1_L
MIC1_R
INT_MIC
ACZ_SDOUT
ACZ_SDIN0
AC97_DATIN
CODECVREF
JDREF
CDAUD_GND
CDAUD_R
CDAUD_L
CD_AGND_R
CD_AUDR_R
CD_AUDL_R
AUD_LOL
AUD_LOR
5VA_SETPIN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO(1/2)
Y4A
Custom
Rev
-1
Tuesday, January 23, 2007
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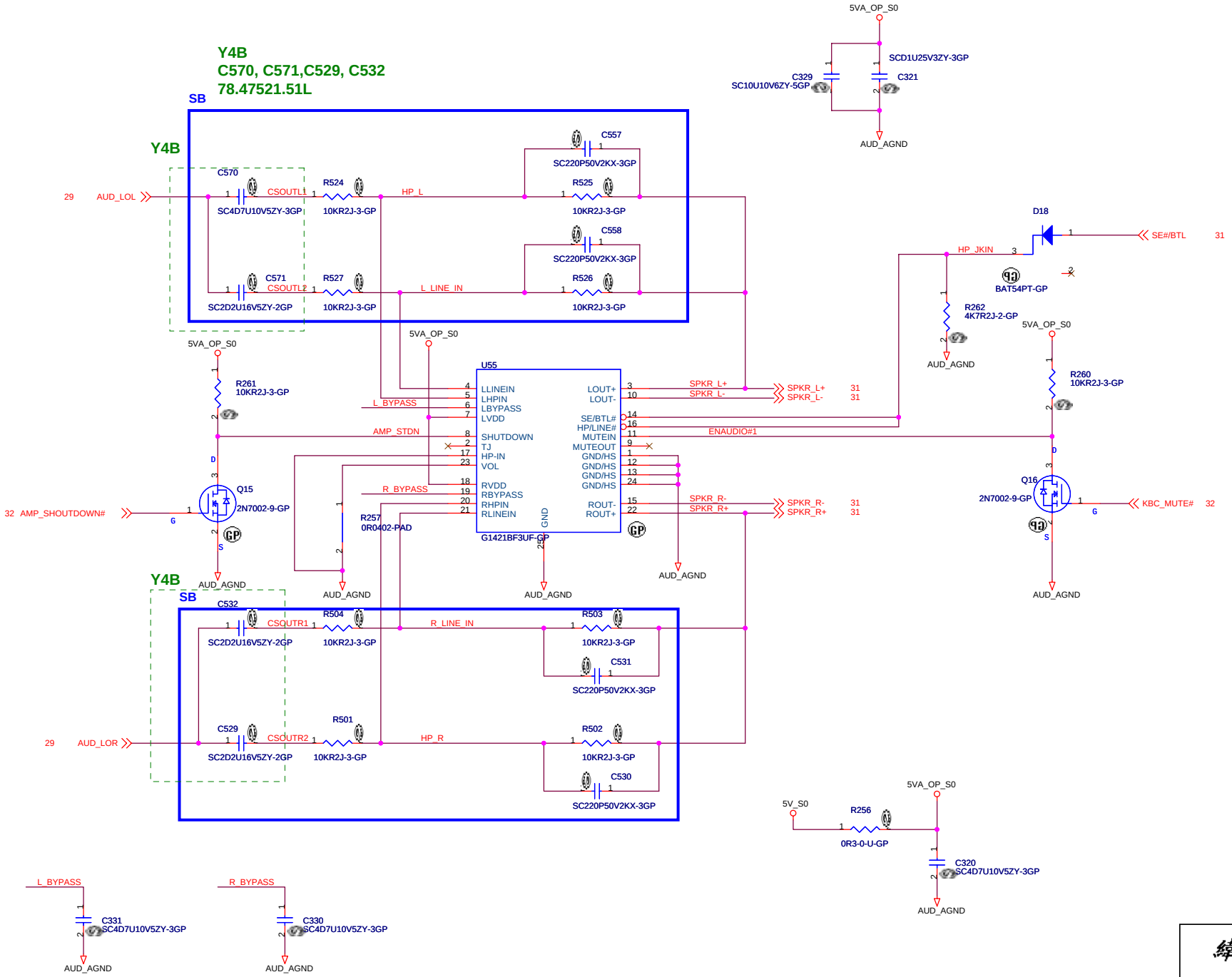
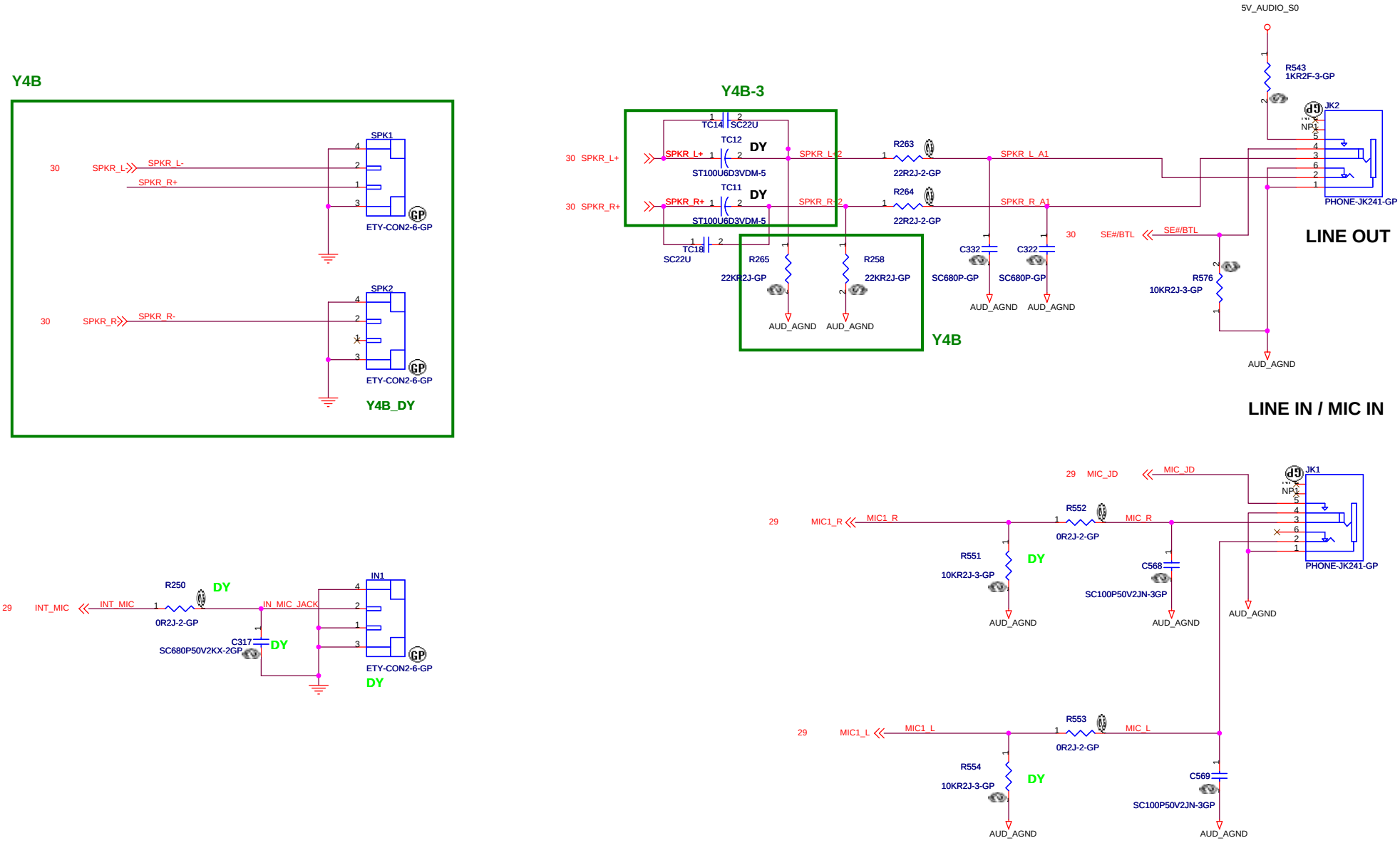
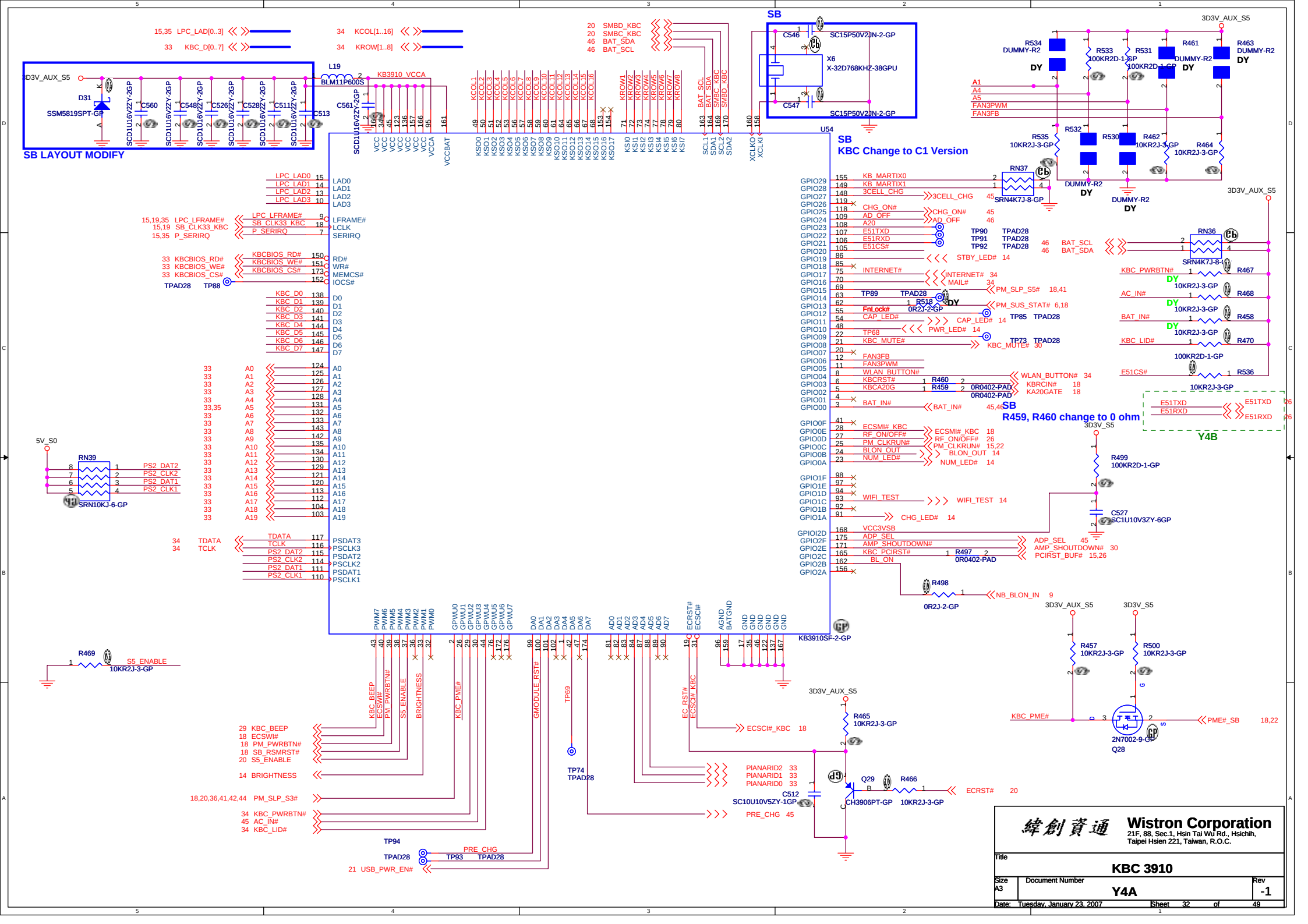


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***AUDIO(2/2)***
Size: A3	Document Number: Y4A
Rev: -1	
Date: Tuesday, January 23, 2007	Sheet 30 of 49



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AUDIO JACK***	
Size A3	Document Number **Y4A**	Rev -1
Date: Tuesday, January 23, 2007	Sheet 31 of 49	


SB
SB LAYOUT MODIFY
SB
KBC Change to C1 Version
SB
R459, R460 change to 0 ohm
Y4B
U54
KB3910SF-2-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC 3910
Size
A3
Document Number
Y4A
Rev
-1
Date: Tuesday, January 23, 2007
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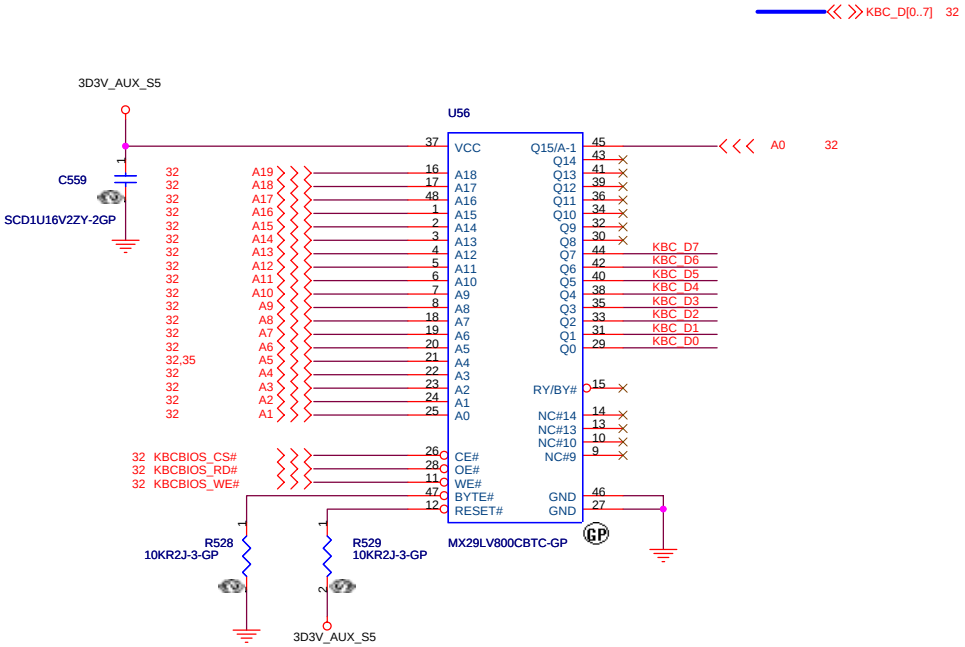
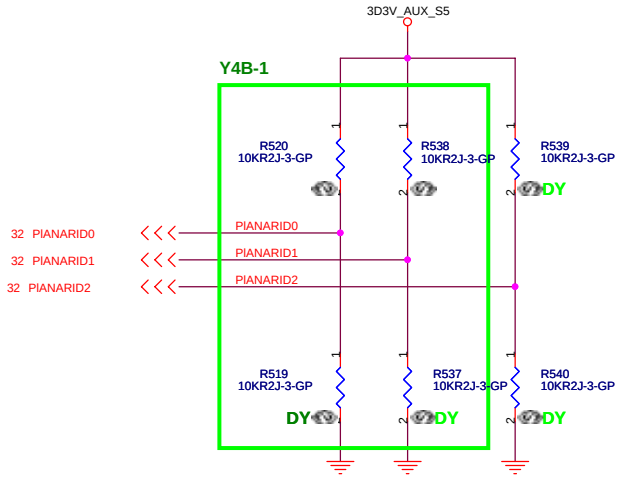


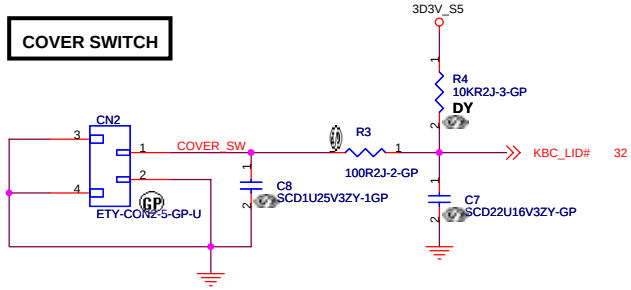


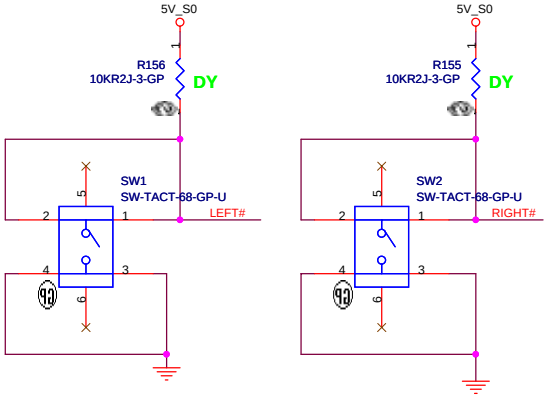
Planar
ID(Resv,1,0)=
Y4A,LAB: Resv,0,0
Y4A,ENG: Resv,0,1
Y4A,PD : Resv,1,0
Y4B,PD : Resv,1,1

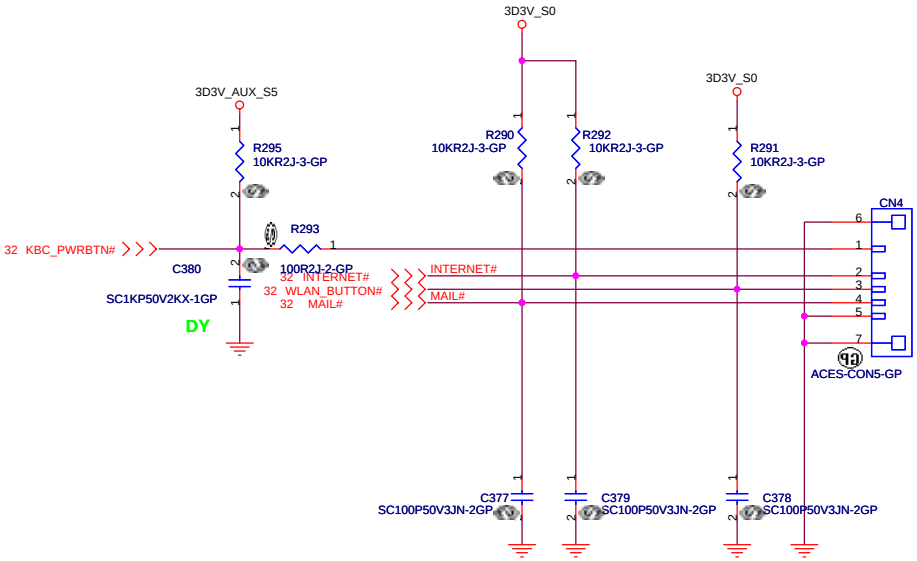
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

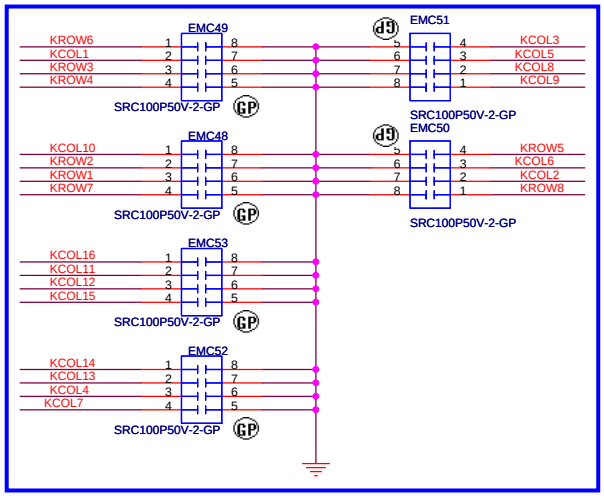
Title: **BIOS ROM**		
Size: A3	Document Number: **Y4A**	Rev: -1
Date: Tuesday, January 23, 2007	Sheet 33 of 49	

Internal KeyBoard Connector

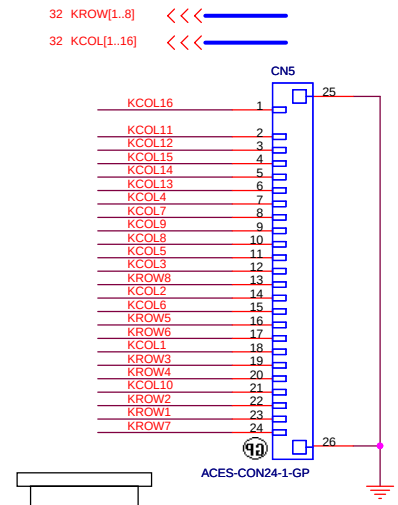




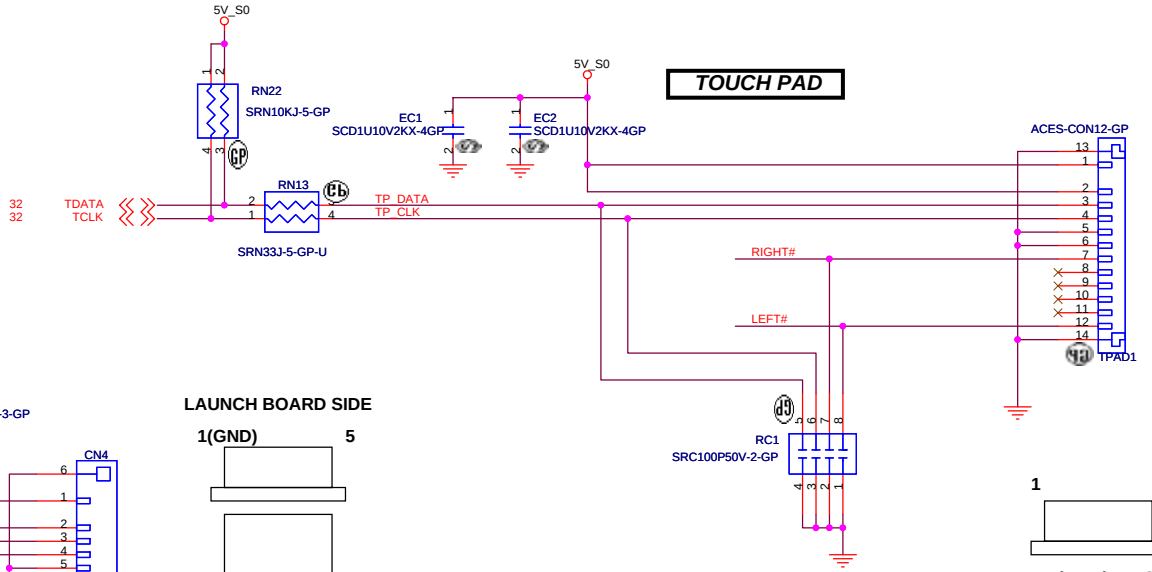


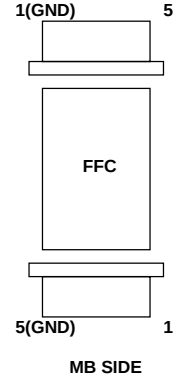


SB



MB PIN DEFINE 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAUNCH / TOUCHPAD / KB CONN	
Size A3	Document Number Y4A	Rev -1
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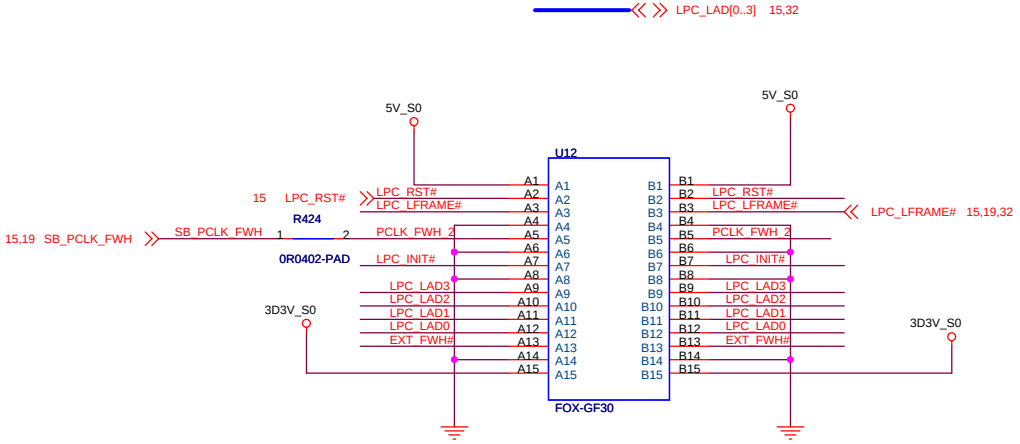
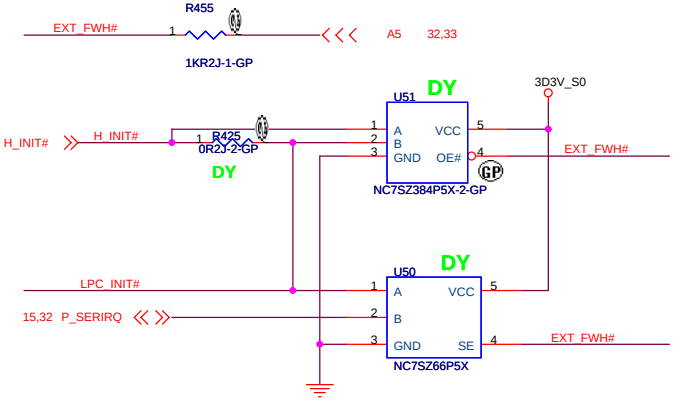
GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

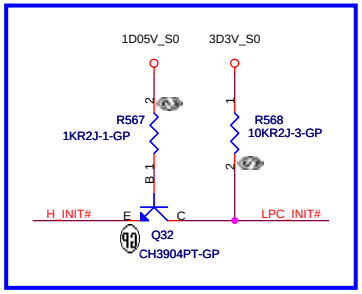
(BOTTOM VIEW)

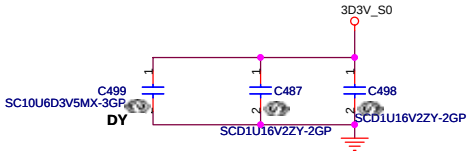




Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SB





緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: Debug (Gold Finger)			
Size: A3	Document Number: Y4A		Rev: -1
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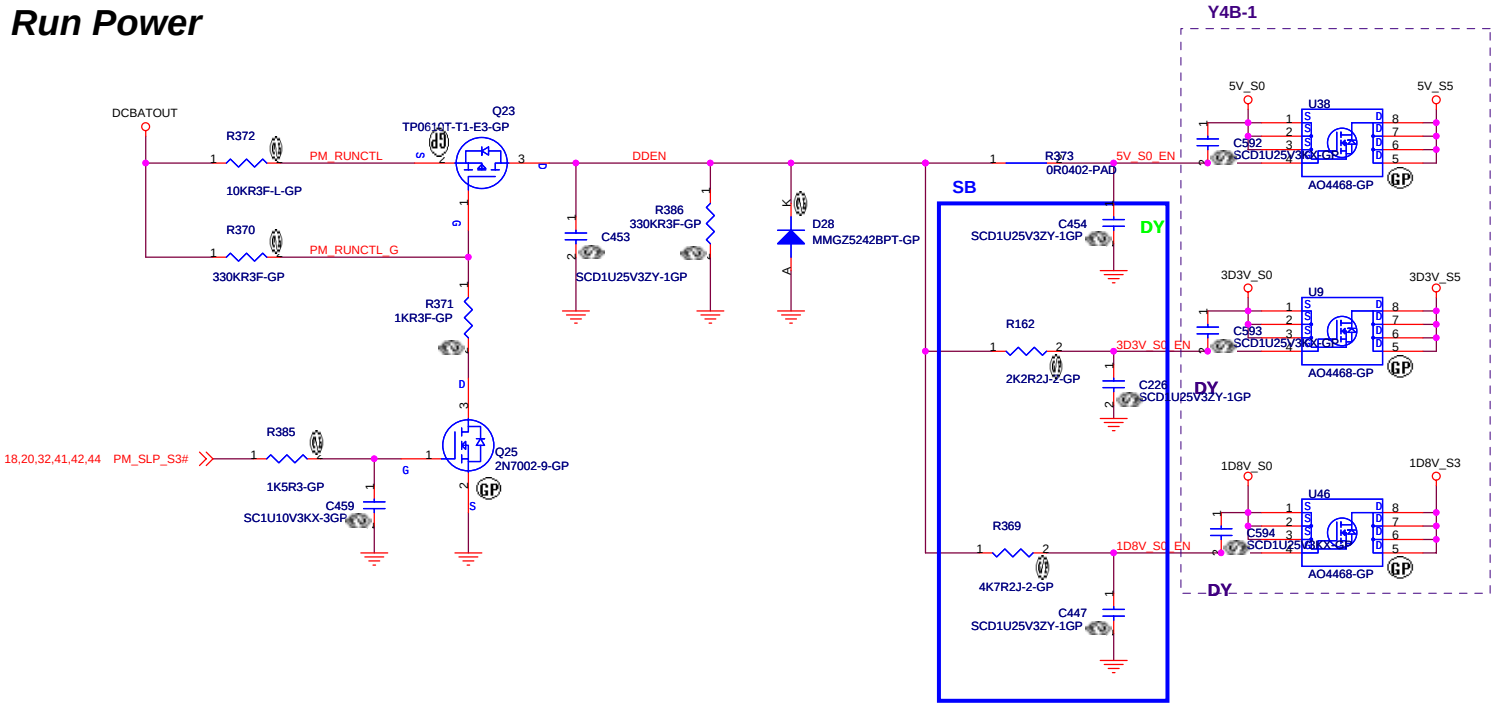
Run Power



Power On Logic

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PWR CTL LOGIC / PWR PLANE		
Size: A3	Document Number: Y4A	Rev: -1
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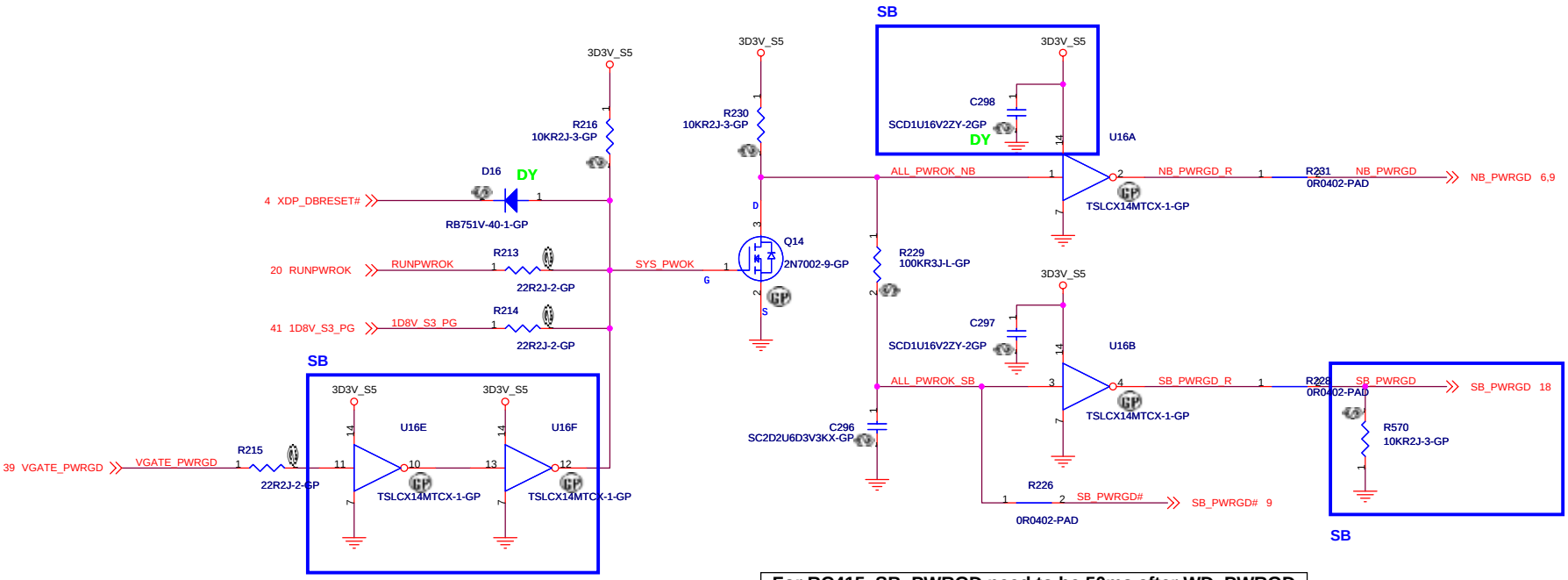
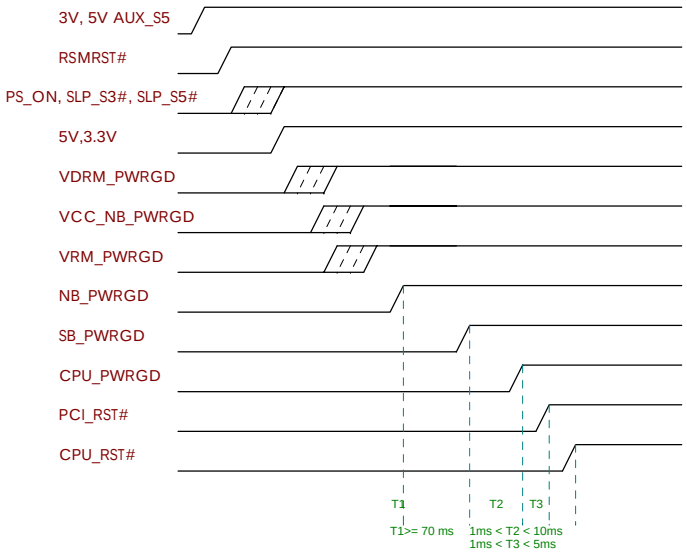
NB_SB POWERGOOD CIRCUIT



For RC415, SB_PWRGD need to be 50ms after WD_PWRGD

ALBACORE POWER UP SEQUENCE



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POWERGOOD&ENABLES(1/2)		
Size: Custom	Document Number: Y4A	Rev: -1
Date: Tuesday, January 23, 2007	Sheet 37 of 49	

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

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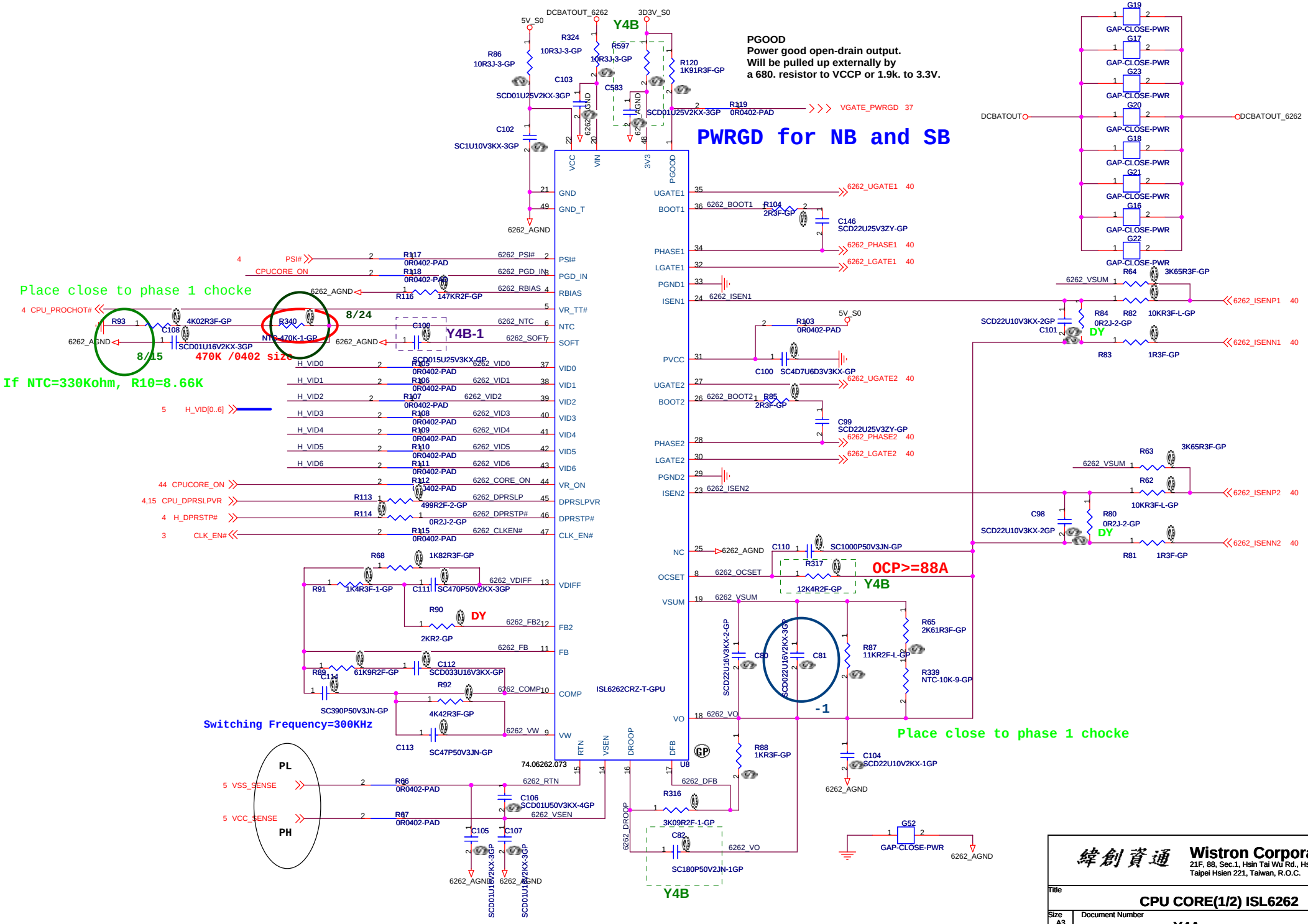
PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
PWRGD for NB and SB
Y4B
Y4B-1
Place close to phase 1 chocke
8/24
8/15
470K /0402 size
If NTC=330Kohm, R10=8.66K
Switching Frequency=300KHz
OCP>=88A
DY
-1
ISL6262CRZ-T-GPU
74.06262.073
PL
PH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU CORE(1/2) ISL6262
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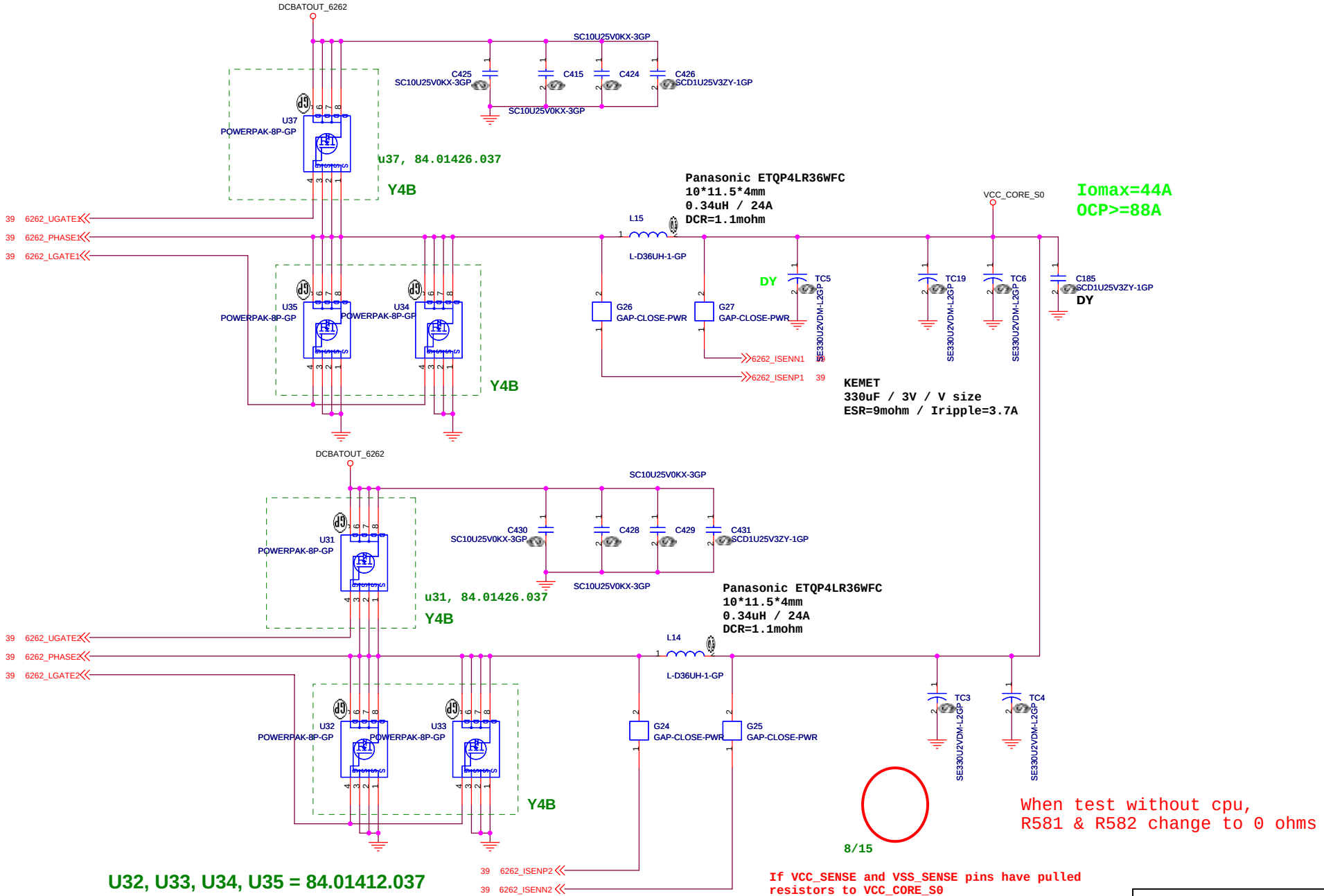

(Power Team)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU CORE(2/2) ISL6262	
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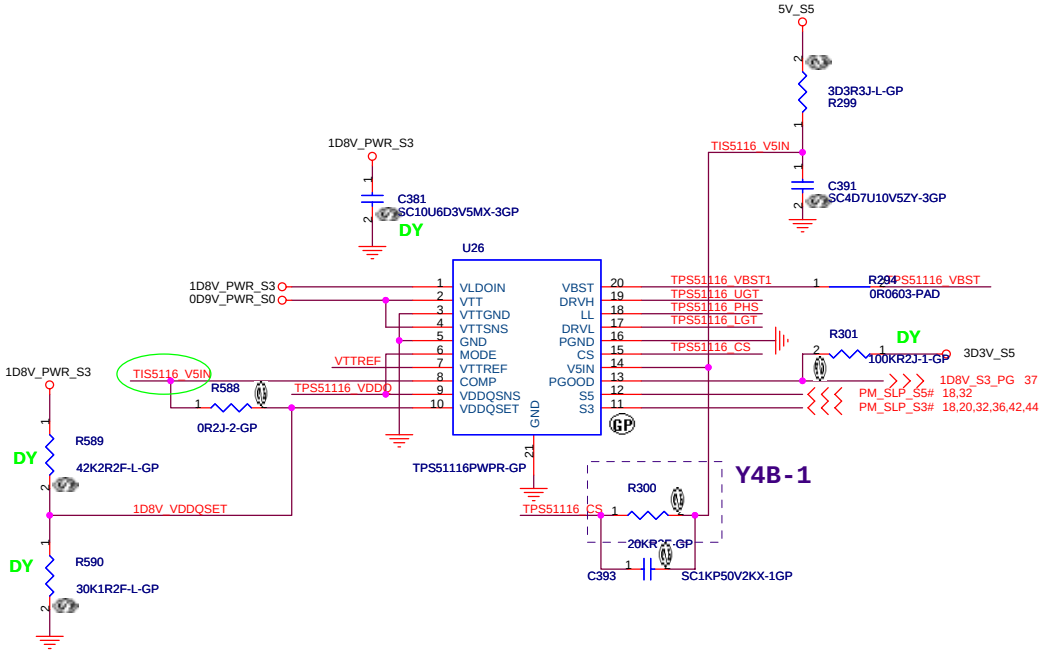
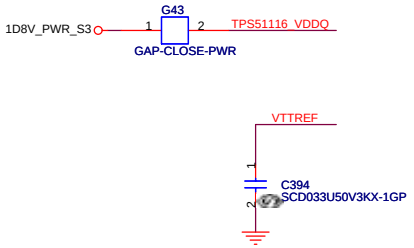
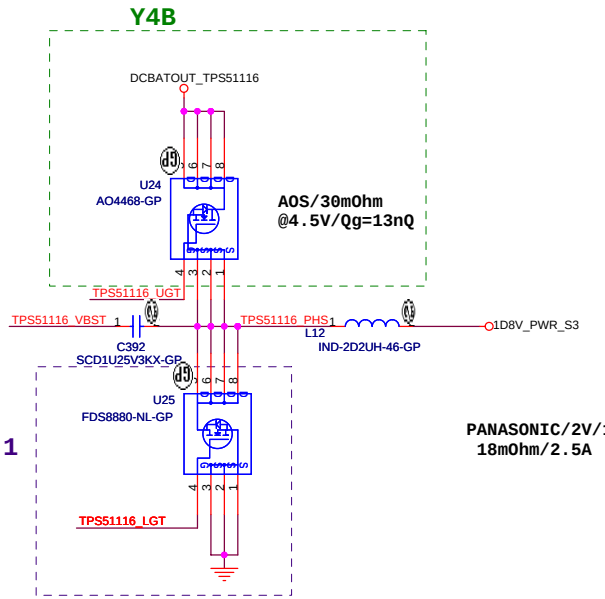
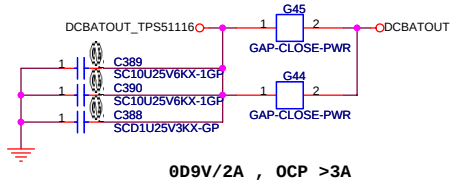
TI TPS51116 for 1D8V and 0D9V

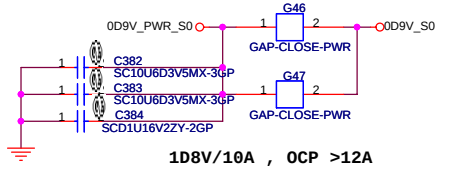




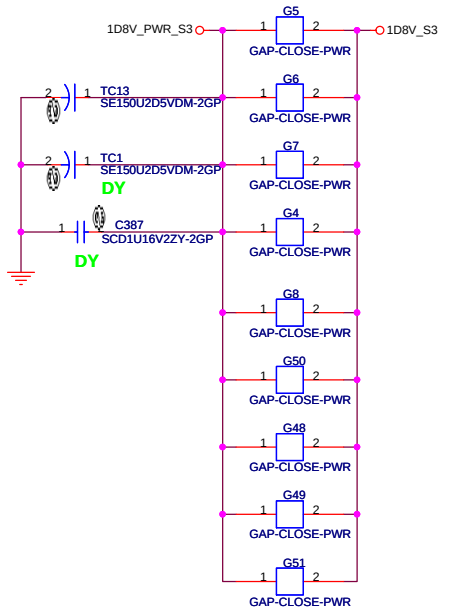




0D9V/2A , OCP >3A



1D8V/10A , OCP >12A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51116 1D8V/0D9V	
Size A3	Document Number Y4A	Rev -1
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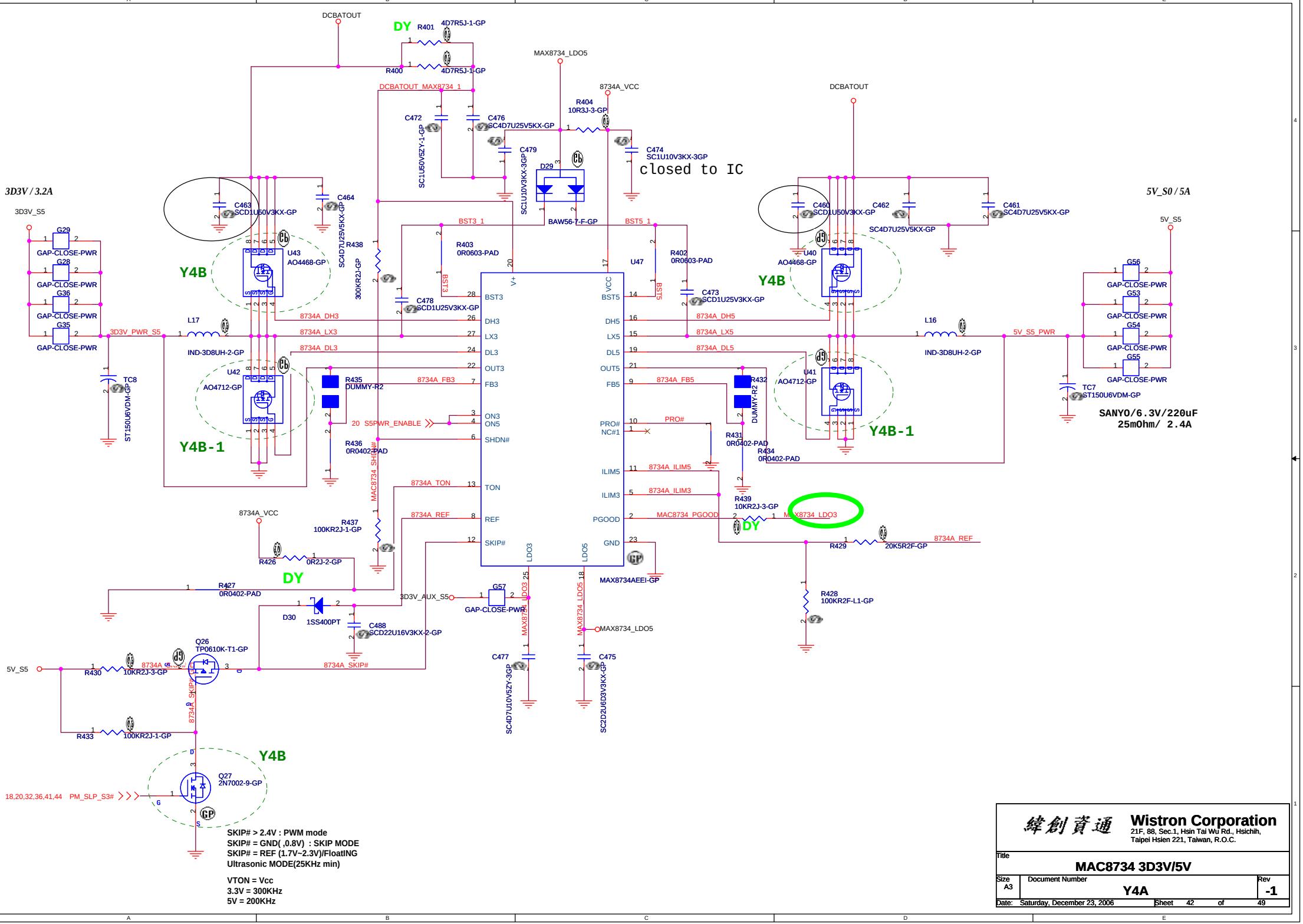
3D3V / 3.2A
5V_S0 / 5A
DCBATOUT
DY
R401 4D7R5J-1-GP
R400 4D7R5J-1-GP
MAX8734_LDO5
8734A_VCC
R404 10R3J-3-GP
DCBATOUT_MAX8734_1
C472 SC1U50V5ZY-1-GP
C476 SC4D7U25V5KX-GP
C479 SC1U10V3KX-3GP
C474 SC1U10V3KX-3GP
closed to IC
D29 BAW56-7-F-GP
C463 SCD1U50V3KX-GP
C464 SC4D7U25V5KX-GP
R438 300KR2J-GP
BST3_1
BST5_1
R403 0R0603-PAD
R402 0R0603-PAD
C478 SCD1U25V3KX-GP
C473 SCD1U25V3KX-GP
U43 AO4468-GP
U47
U40 AO4468-GP
C460 SCD1U50V3KX-GP
C462 SC4D7U25V5KX-GP
C461 SC4D7U25V5KX-GP
Y4B
3D3V_S5
G29 GAP-CLOSE-PWR
G28 GAP-CLOSE-PWR
G36 GAP-CLOSE-PWR
G35 GAP-CLOSE-PWR
L17 IND-3D8UH-2-GP
3D3V_PWR_S5
TC8 ST150U6VDM-GP
8734A_DH3
8734A_LX3
8734A_DL3
U42 AO4712-GP
R435 DUMMY-R2
8734A_FB3
20 S5PWR_ENABLE
R436 0R0402-PAD
MAC8734_SHDN#
Y4B-1
8734A_TON
8734A_REF
R437 100KR2J-1-GP
8734A_VCC
R426 0R2J-2-GP
DY
R427 0R0402-PAD
D30 1SS400PT
3D3V_AUX_S5
G57 GAP-CLOSE-PWR
C488 SCD22U16V3KX-2-GP
Q26 TP0610K-T1-GP
5V_S5
R430 10KR2J-3-GP
8734A_SKIP#
R433 100KR2J-1-GP
Q27 2N7002-9-GP
18,20,32,36,41,44 PM_SLP_S3#
BST3
DH3
LX3
DL3
OUT3
FB3
ON3
ON5
SHDN#
TON
REF
SKIP#
V+
VCC
BST5
DH5
LX5
DL5
OUT5
FB5
PRO#
NC#1
ILIM5
ILIM3
PGOOD
GND
LDO3
LDO5
MAX8734AEEI-GP
MAX8734_LDO3
MAX8734_LDO5
C477 SC4D7U10V5ZY-3GP
C475 SC2D2U6D3VKX-GP
U41 AO4712-GP
R432 DUMMY-R2
8734A_FB5
PRO#
R431 0R0402-PAD
R434 0R0402-PAD
8734A_ILIM5
8734A_ILIM3
R439 10KR2J-3-GP
MAC8734_PGOOD
DY
R429 20K5R2F-GP
R428 100KR2F-L1-GP
L16 IND-3D8UH-2-GP
5V_S5_PWR
G56 GAP-CLOSE-PWR
G53 GAP-CLOSE-PWR
G54 GAP-CLOSE-PWR
G55 GAP-CLOSE-PWR
TC7 ST150U6VDM-GP
SANYO/6.3V/220uF
25mOhm/ 2.4A
SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V~2.3V)/FloatING
Ultrasonic MODE(25KHz min)
VTON = Vcc
3.3V = 300KHz
5V = 200KHz
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAC8734 3D3V/5V
Size A3
Document Number
Y4A
Rev -1
Date: Saturday, December 23, 2006
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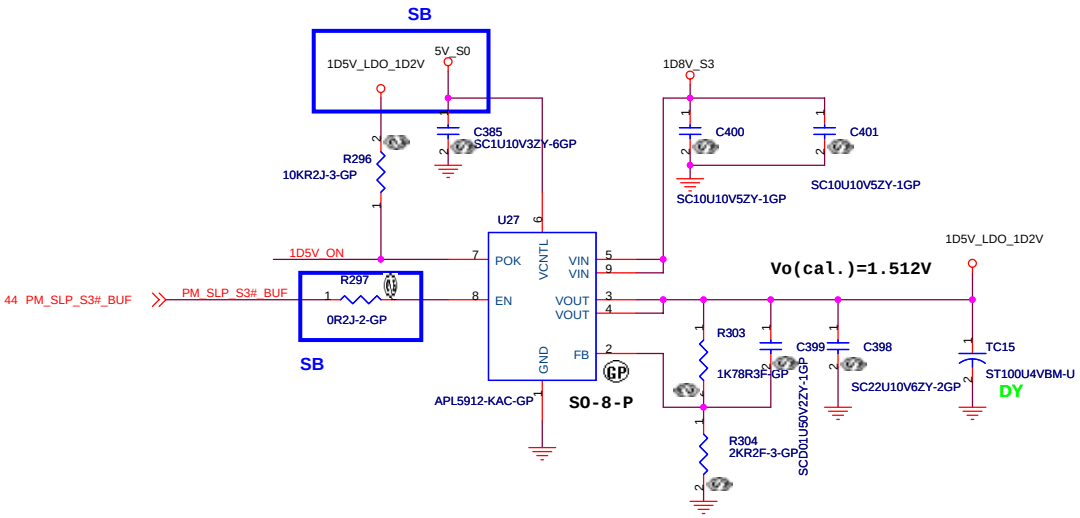
NB CORE 1.2V

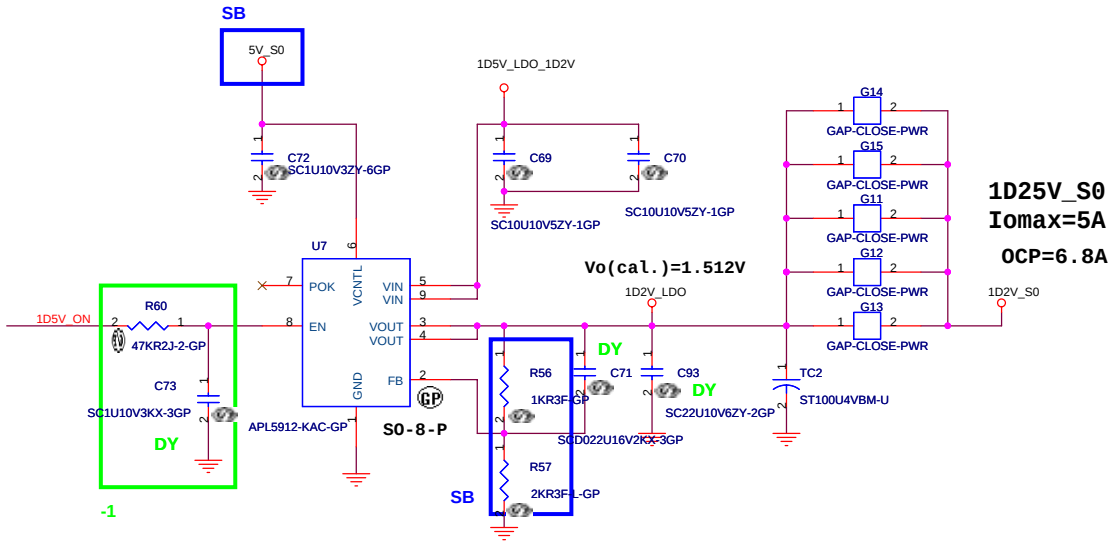
1D8V to 1D5V



1D5V_LDO_1D2V
Iomax=5A

Vo=0.8*(1+(R1/R2))

1D5V to 1D2V

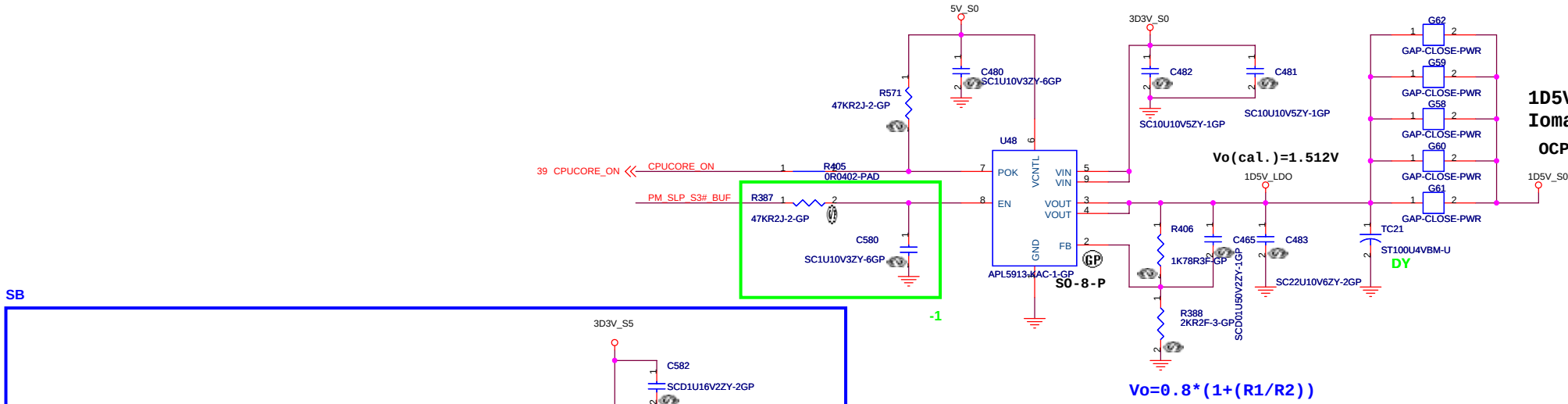


1D25V_S0
Iomax=5A
OCP=6.8A

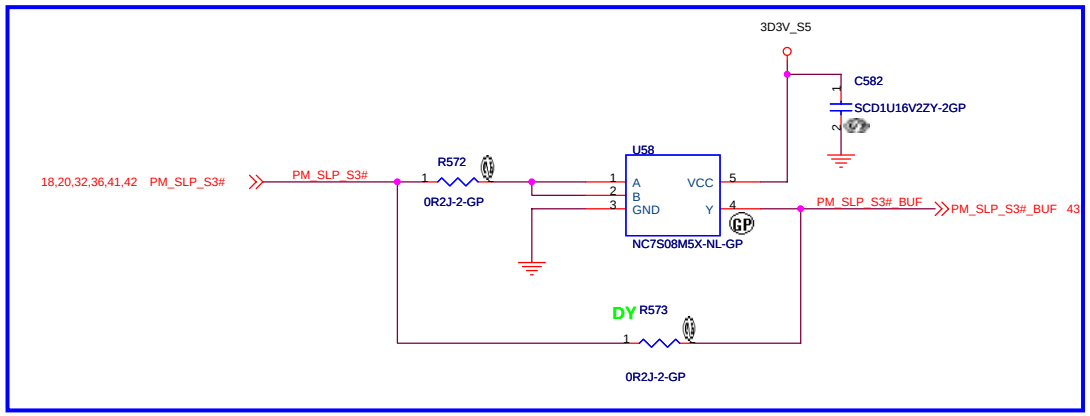
Vo=0.8*(1+(R1/R2))

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: 39.DC/DC 5V/3D3V/1D2V-2		
Size: A3	Document Number: Y4A	Rev: -1
Date: Tuesday, January 23, 2007	Sheet 43 of 49	

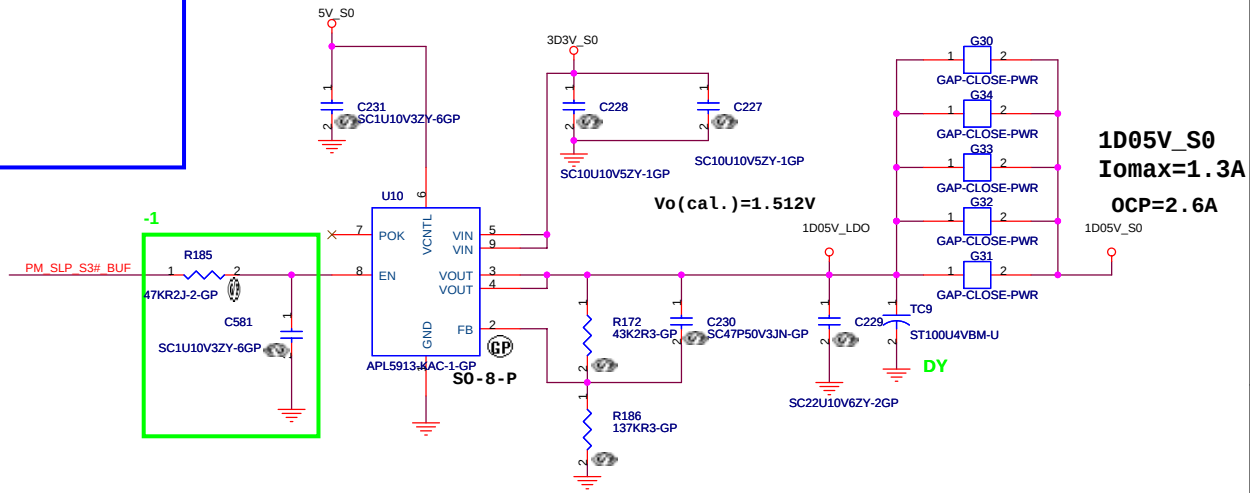
1D5V_LDO FOR NEW CARD



SB

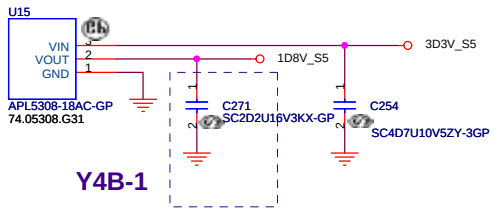


1D05V FOR CPU VCCP



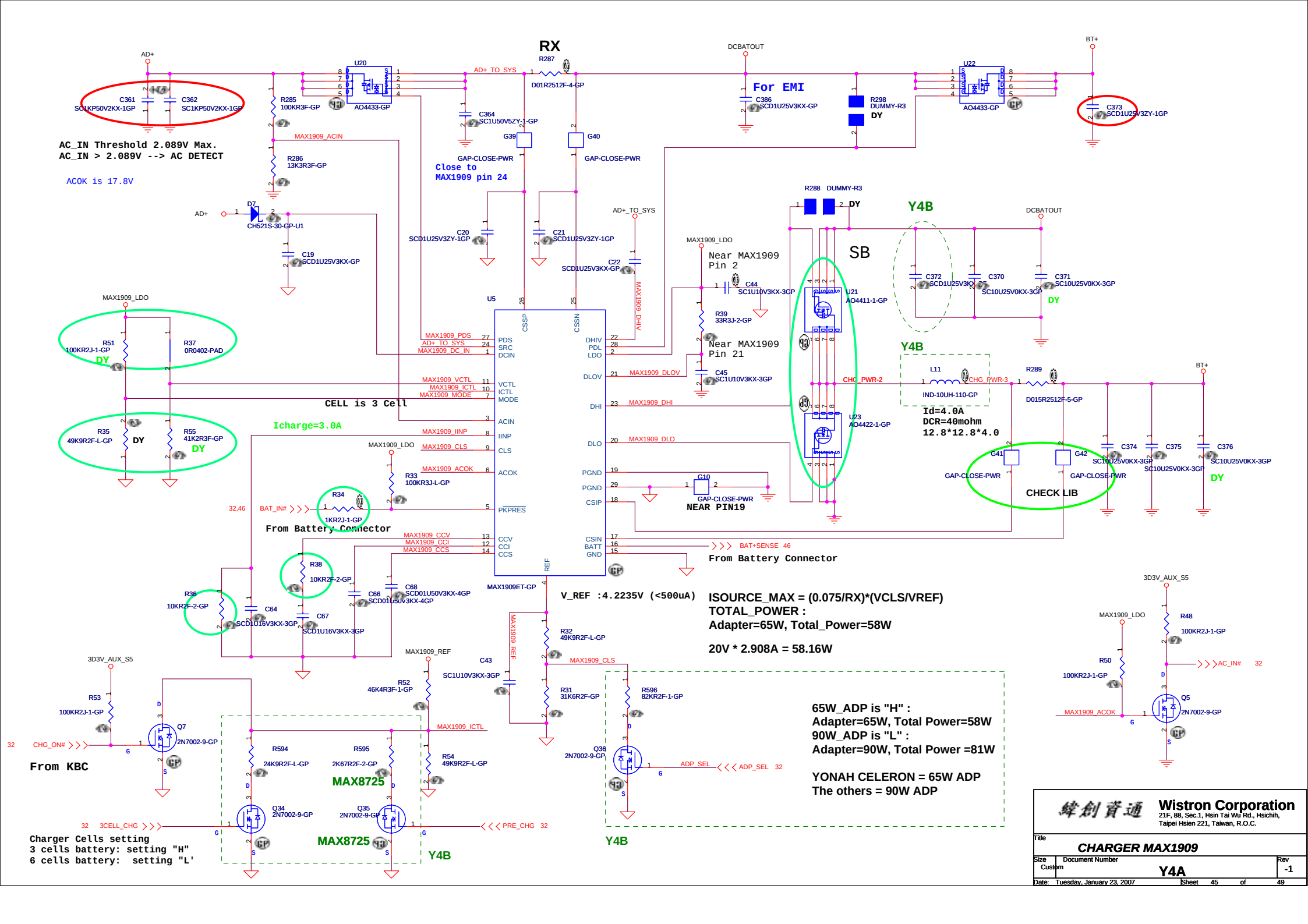
1D8V_S5

MAX. = 300mA



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*2D5V/3D3V_AUX/5V_AUX/1D5V*
Size: A3	Document Number: Y4A — Rev: -1
Date: Tuesday, January 23, 2007	Sheet 44 of 49


RX
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
Close to MAX1909 pin 24
For EMI
SB
Y4B
Near MAX1909 Pin 2
Near MAX1909 Pin 21
CELL is 3 Cell
Icharge=3.0A
From Battery Connector
From Battery Connector
NEAR PIN19
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/RX)*(VCLS/VREF)
TOTAL_POWER :
Adapter=65W, Total_Power=58W
20V * 2.908A = 58.16W
Id=4.0A
DCR=40mohm
12.8*12.8*4.0
CHECK LIB
From KBC
MAX8725
MAX8725
Y4B
Y4B
65W_ADP is "H" :
Adapter=65W, Total Power=58W
90W_ADP is "L" :
Adapter=90W, Total Power =81W
YONAH CELERON = 65W ADP
The others = 90W ADP
Charger Cells setting
3 cells battery: setting "H"
6 cells battery: setting "L'
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CHARGER MAX1909
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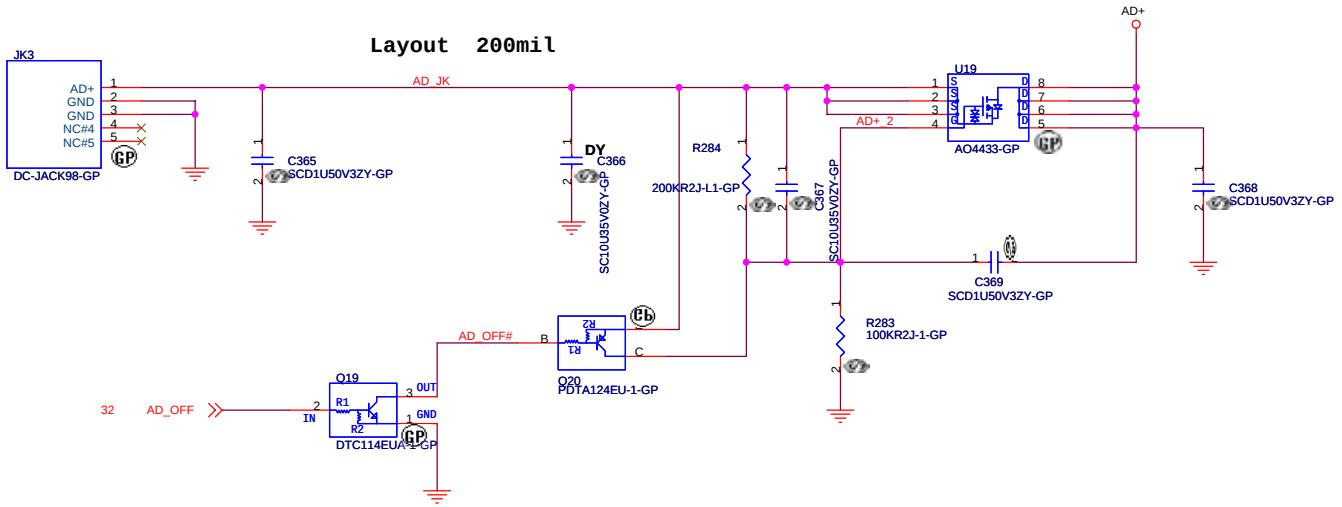
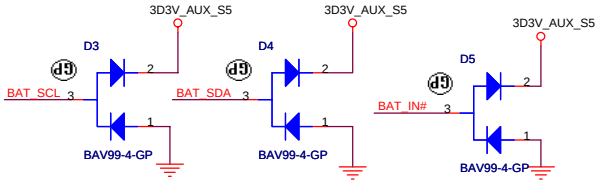
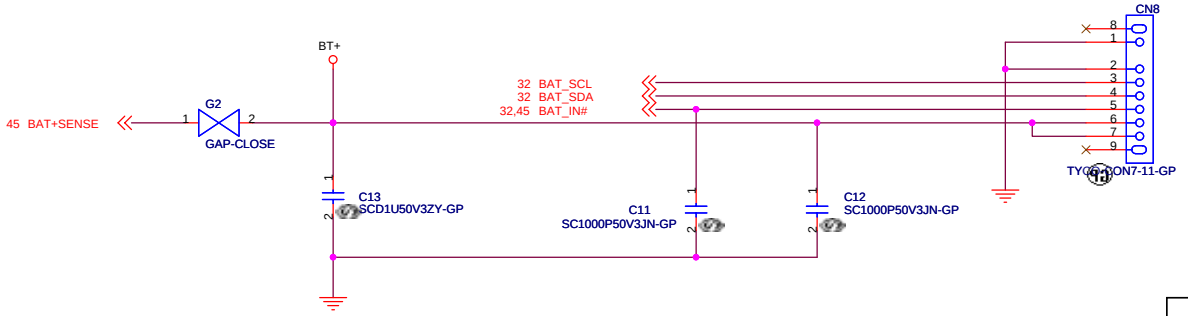
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





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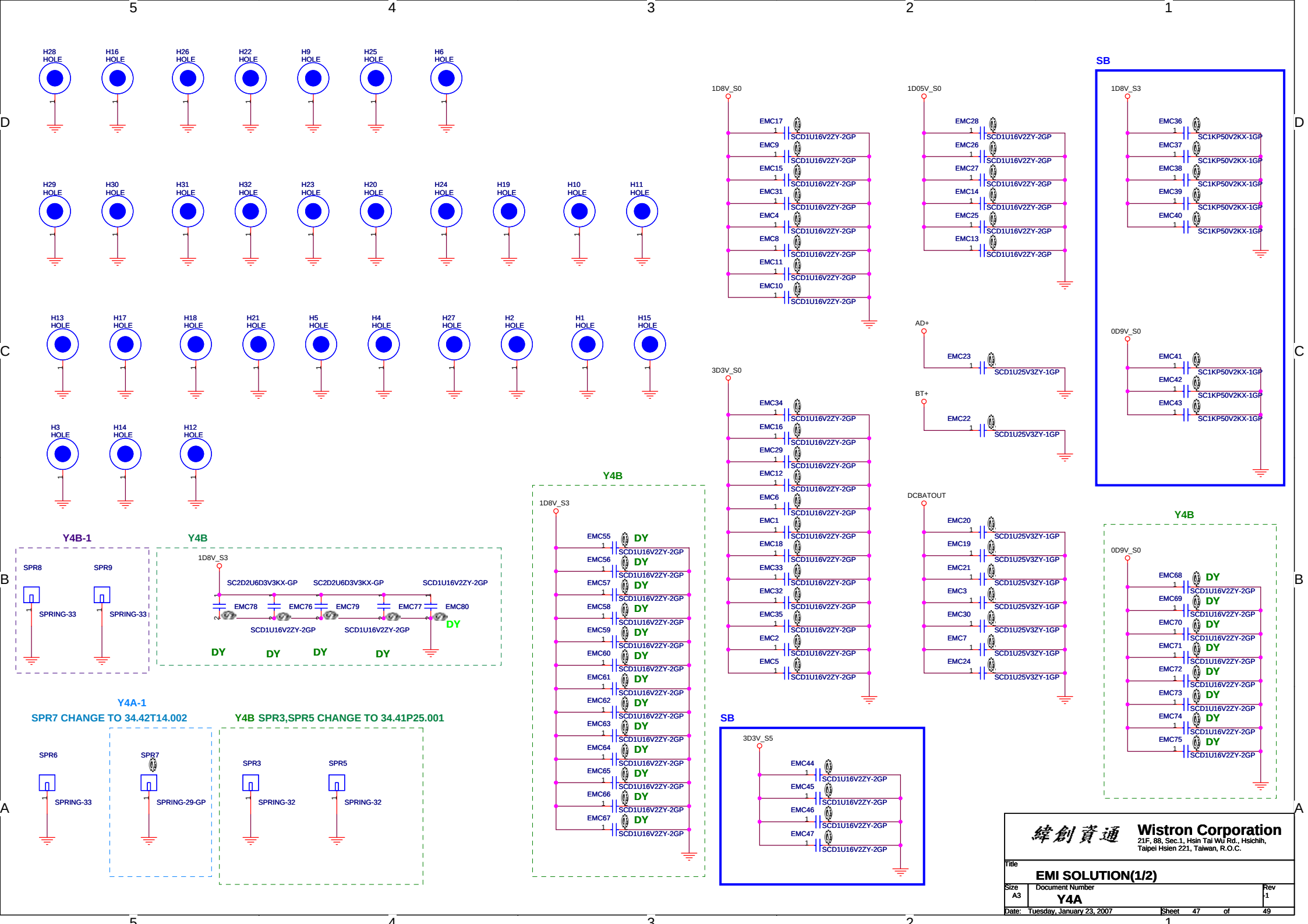
H28 HOLE
H16 HOLE
H26 HOLE
H22 HOLE
H9 HOLE
H25 HOLE
H6 HOLE
H29 HOLE
H30 HOLE
H31 HOLE
H32 HOLE
H23 HOLE
H20 HOLE
H24 HOLE
H19 HOLE
H10 HOLE
H11 HOLE
H13 HOLE
H17 HOLE
H18 HOLE
H21 HOLE
H5 HOLE
H4 HOLE
H27 HOLE
H2 HOLE
H1 HOLE
H15 HOLE
H3 HOLE
H14 HOLE
H12 HOLE
Y4B-1
SPR8
SPR9
SPRING-33
SPRING-33
Y4B
1D8V_S3
SC2D2U6D3V3KX-GP
SC2D2U6D3V3KX-GP
SCD1U16V2ZY-2GP
EMC78
EMC76
EMC79
EMC77
EMC80
SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
DY
DY
DY
DY
DY
Y4A-1
SPR7 CHANGE TO 34.42T14.002
Y4B SPR3,SPR5 CHANGE TO 34.41P25.001
SPR6
SPR7
SPRING-33
SPRING-29-GP
SPR3
SPR5
SPRING-32
SPRING-32
Y4B
1D8V_S3
EMC55 DY SCD1U16V2ZY-2GP
EMC56 DY SCD1U16V2ZY-2GP
EMC57 DY SCD1U16V2ZY-2GP
EMC58 DY SCD1U16V2ZY-2GP
EMC59 DY SCD1U16V2ZY-2GP
EMC60 DY SCD1U16V2ZY-2GP
EMC61 DY SCD1U16V2ZY-2GP
EMC62 DY SCD1U16V2ZY-2GP
EMC63 DY SCD1U16V2ZY-2GP
EMC64 DY SCD1U16V2ZY-2GP
EMC65 DY SCD1U16V2ZY-2GP
EMC66 DY SCD1U16V2ZY-2GP
EMC67 DY SCD1U16V2ZY-2GP
1D8V_S0
EMC17 SCD1U16V2ZY-2GP
EMC9 SCD1U16V2ZY-2GP
EMC15 SCD1U16V2ZY-2GP
EMC31 SCD1U16V2ZY-2GP
EMC4 SCD1U16V2ZY-2GP
EMC8 SCD1U16V2ZY-2GP
EMC11 SCD1U16V2ZY-2GP
EMC10 SCD1U16V2ZY-2GP
3D3V_S0
EMC34 SCD1U16V2ZY-2GP
EMC16 SCD1U16V2ZY-2GP
EMC29 SCD1U16V2ZY-2GP
EMC12 SCD1U16V2ZY-2GP
EMC6 SCD1U16V2ZY-2GP
EMC1 SCD1U16V2ZY-2GP
EMC18 SCD1U16V2ZY-2GP
EMC33 SCD1U16V2ZY-2GP
EMC32 SCD1U16V2ZY-2GP
EMC35 SCD1U16V2ZY-2GP
EMC2 SCD1U16V2ZY-2GP
EMC5 SCD1U16V2ZY-2GP
SB
3D3V_S5
EMC44 SCD1U16V2ZY-2GP
EMC45 SCD1U16V2ZY-2GP
EMC46 SCD1U16V2ZY-2GP
EMC47 SCD1U16V2ZY-2GP
1D05V_S0
EMC28 SCD1U16V2ZY-2GP
EMC26 SCD1U16V2ZY-2GP
EMC27 SCD1U16V2ZY-2GP
EMC14 SCD1U16V2ZY-2GP
EMC25 SCD1U16V2ZY-2GP
EMC13 SCD1U16V2ZY-2GP
AD+
EMC23 SCD1U25V3ZY-1GP
BT+
EMC22 SCD1U25V3ZY-1GP
DCBATOUT
EMC20 SCD1U25V3ZY-1GP
EMC19 SCD1U25V3ZY-1GP
EMC21 SCD1U25V3ZY-1GP
EMC3 SCD1U25V3ZY-1GP
EMC30 SCD1U25V3ZY-1GP
EMC7 SCD1U25V3ZY-1GP
EMC24 SCD1U25V3ZY-1GP
SB
1D8V_S3
EMC36 SC1KP50V2KX-1GP
EMC37 SC1KP50V2KX-1GP
EMC38 SC1KP50V2KX-1GP
EMC39 SC1KP50V2KX-1GP
EMC40 SC1KP50V2KX-1GP
0D9V_S0
EMC41 SC1KP50V2KX-1GP
EMC42 SC1KP50V2KX-1GP
EMC43 SC1KP50V2KX-1GP
Y4B
0D9V_S0
EMC68 DY SCD1U16V2ZY-2GP
EMC69 DY SCD1U16V2ZY-2GP
EMC70 DY SCD1U16V2ZY-2GP
EMC71 DY SCD1U16V2ZY-2GP
EMC72 DY SCD1U16V2ZY-2GP
EMC73 DY SCD1U16V2ZY-2GP
EMC74 DY SCD1U16V2ZY-2GP
EMC75 DY SCD1U16V2ZY-2GP
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Wistron Corporation
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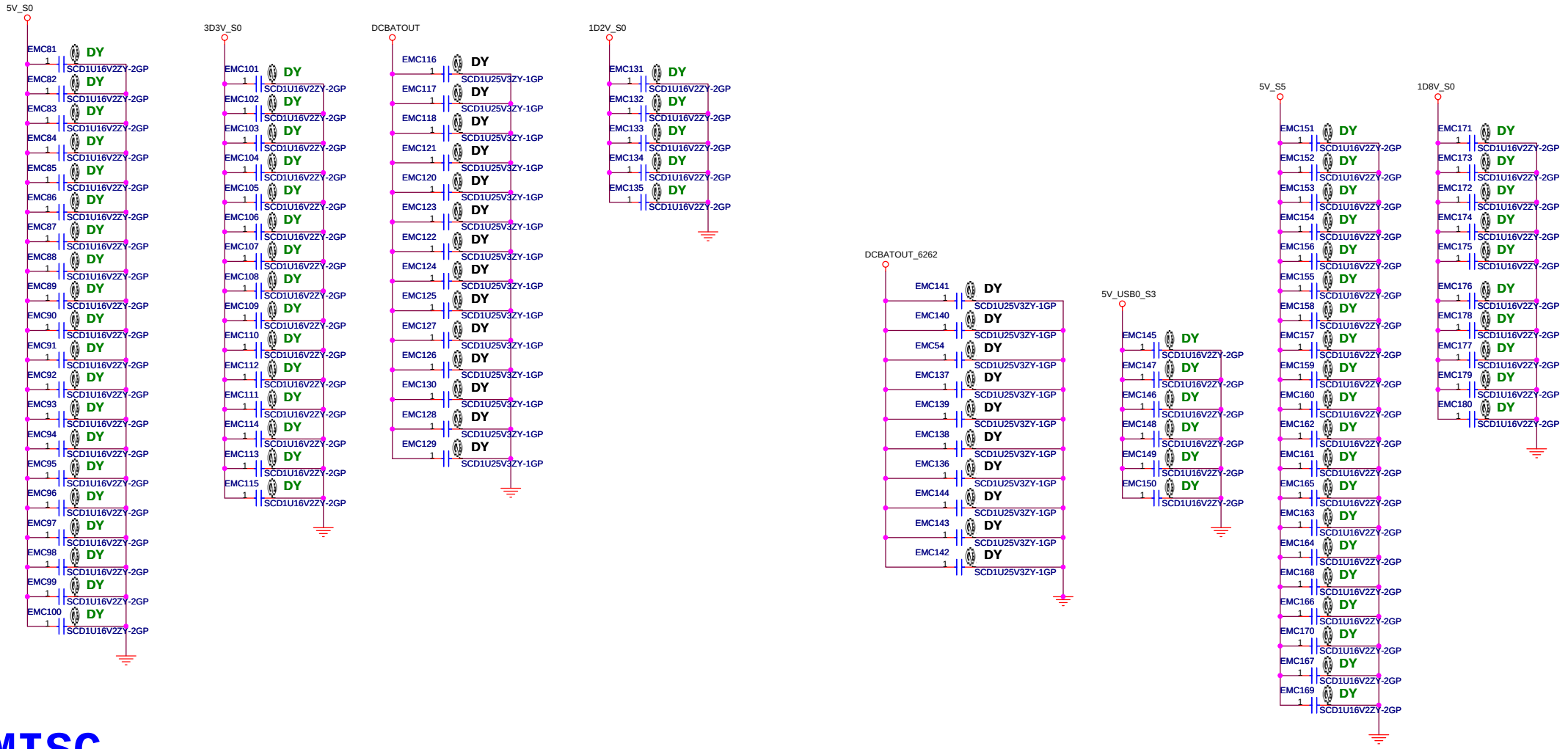
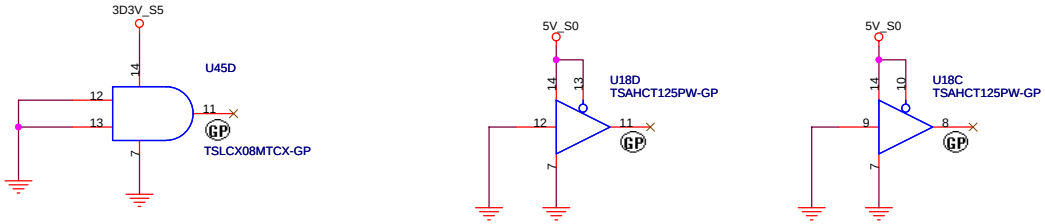
EMI



MISC



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PRT modification list for Layout:

CN10, SPD-CONN50-4R-14GP-U , K211-CB02A50R
U29, SKT-SODIMM20020U3GP, 1717254-4
U36, BGA479-SKT6-GPU3, BGA479-SKT-6H209U3

PRT modification list for Y4A BOM:

U28, 71.RC415.M01(version A11)
C570,C571,C532,C529, 78.47521.51L(second source: 78.47522.51L)
U57, 71.AL861.A0G(version D)
U31,U37, 84.01426.037
U32,U33,U34,U35, 84.01412.037
U49, 71.SB460.M04(version A12)
SPR7, 34.42T14.002
U29, 62.10017.A41
XF1, 68.0H80P.30A
MINIC1, 62.10043.261
SPR3,SPR5, 34.41P25.001
CN10, 20.80361.050

銅柱:
H1,H12,H20,H23,H29,H30, 34.46I14.001
H4,H5, 34.4B604.001
H31,H32, 34.4B601.001

If U5 is P/N:74.01909.A74, DY R595(P/N:64.26715.6DL) and Q35(P/N:84.27002.J11)
If U5 is P/N:74.08725.A73, Add R595(P/N:64.26715.6DL) and Q35(P/N:84.27002.J11)

<Variant Name>

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Title: Remark

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