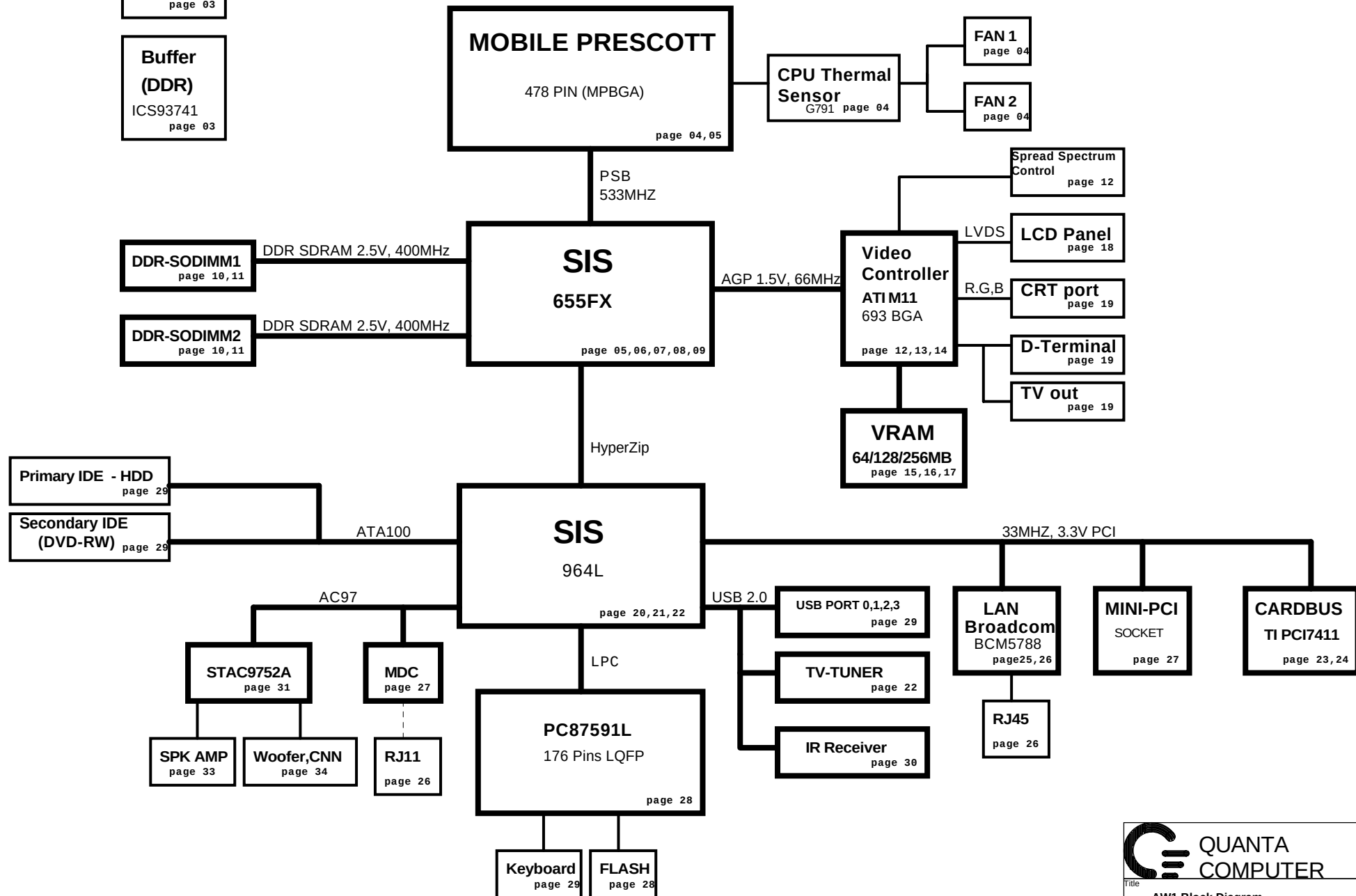


AW1 BLOCK DIAGRAM

Mobile Prescott & SIS655FX



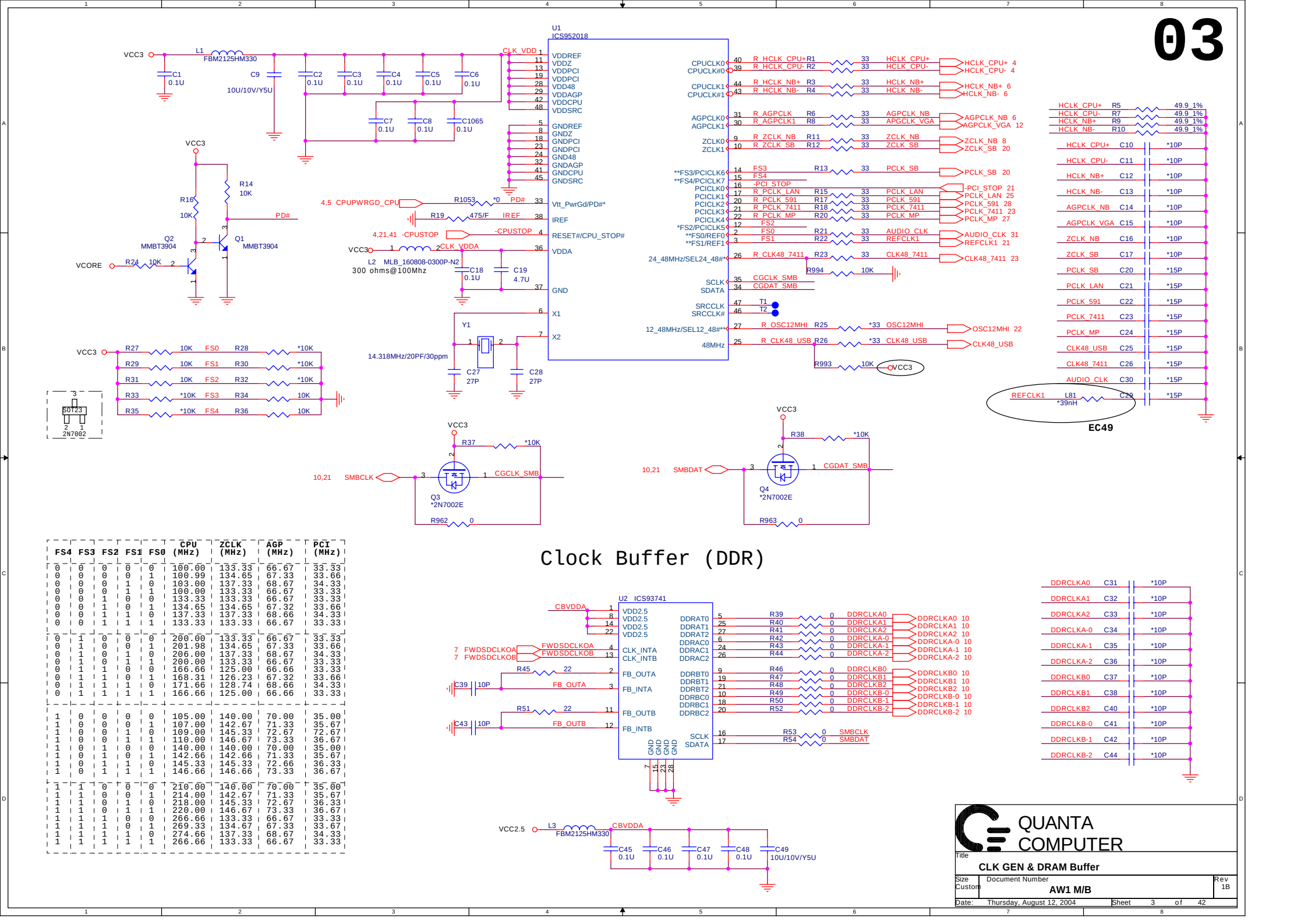
AW1 Schematic Page Description :

02

01--BLOCK DIAGRAM
02--Schematic Sheet Number
03--CLOCK GENERATOR
04--Mobile Prescott CPU-1
05--Mobile Prescott CPU-2
06--NB(655FX HOST & AGP)
07--NB(655FX UMCA&B)
08--NB(655FX LINK)
09--NB(655FX POWER)
10--SYSTEM DIMM1&2
11--DDR_TERMINASION
12--VGA(M11-P AGP INTERFACE)
13--VGA(M11-P MEM A&B)
14--VGA(M11-P PWR&GROUN)
15--VGA(VIDEO MEM A)
16--VGA(VIDEO MEM B)
17--VGA(TERMINATION & VGA ROM)
18--PANEL I/F,LED
19--CRT&S-VIDEO
20--964L-1 PCI/IDE/Link.SCH
21--964L-2 LPC/MII/CPU/GPIO.SCH
22--964L-3 USB/SATA.SCH
23--PCI7411 PCMCIA CONTROLLER
24--PCMCIA CNN & 3 IN 1
25--LAN (BCM5788-10/100/GIGA)

26--LAN (TR & CONNECTOR)
27--MINI-PCI/MDC
28--PCU-87591 & FLASH
29--K/B,USB,HDD,CDROM
30--RTC,BEEP,T/P,BUTTON,RECEIVE
31--AUDIO(STAC9752A,MIC CON)
32--AUDIO(AMP & POWER & HP CON)
33--AUDIO (Power AMP, SP CON)
34--AUDIO (Sub Woofer AMP)
35--1.5V/1.8V/2.5V & DDRVTT
36--VGA POWER
37--DC/DC 3V/5V
38--BATTERY CHARGER
39--BATTERY CONNECTOR
40--CPU POWER-1
41--CPU POWER-2

 QUANTA COMPUTER			
Title AW1 Block Diagram			
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03

The schematic diagram illustrates the clock generation and buffer circuitry for a system. It features several key components and sections:

- Voltage Regulation:** A VCC3 regulator section at the top left includes a feedback network with resistors R14, R16, and R18, and capacitors C1, C2, C3, C4, C5, C6, C7, C8, and C1065.
- Clock Sources:** Two main clock sources are shown: a 14.318MHz/20PF/30ppm crystal (Y1) and a 12_48MHz/SEL12_48M# oscillator (U2).
- Signal Buffers:** Multiple buffers are used to drive various signals, including CPUCLK0, CPUCLK1, AGPCLK0, AGPCLK1, ZCLK0, ZCLK1, PCLK_SB, PCLK_LAN, PCLK_591, PCLK_MP, CLK48_USB, CLK48_7411, AUDIO_CLK, REFCLK1, and DDRCLKA0 through DDRCLKB2.
- Timing and Delay Elements:** Various delay elements are specified, such as *10P, *15P, *100P, and *39nH.
- Component Values:** Resistor values range from 0.1K to 10K, and capacitor values range from 0.1uF to 10uF.

Signal	FS4	FS3	FS2	FS1	FS0	CPU (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
0	0	0	0	0	0	100.00	133.33	66.67	33.33
0	0	0	0	0	1	100.99	134.65	67.33	33.66
0	0	0	0	1	0	103.00	137.33	68.67	34.33
0	0	0	1	0	0	100.00	133.33	66.67	33.33
0	0	0	1	0	1	103.00	137.33	68.67	34.33
0	0	1	0	0	0	100.00	133.33	66.67	33.33
0	0	1	0	1	0	103.00	137.33	68.67	34.33
0	0	1	1	0	0	100.00	133.33	66.67	33.33
0	0	1	1	0	1	103.00	137.33	68.67	34.33
0	0	1	1	1	0	100.00	133.33	66.67	33.33
0	0	1	1	1	1	103.00	137.33	68.67	34.33
1	0	0	0	0	0	105.00	140.00	70.00	35.00
1	0	0	0	0	1	107.00	142.67	71.33	35.67
1	0	0	0	1	0	109.00	145.33	72.67	36.33
1	0	0	0	1	1	110.00	146.67	73.33	36.67
1	0	0	1	0	0	105.00	140.00	70.00	35.00
1	0	0	1	0	1	107.00	142.67	71.33	35.67
1	0	0	1	1	0	109.00	145.33	72.67	36.33
1	0	0	1	1	1	110.00	146.67	73.33	36.67
1	0	1	0	0	0	105.00	140.00	70.00	35.00
1	0	1	0	0	1	107.00	142.67	71.33	35.67
1	0	1	0	1	0	109.00	145.33	72.67	36.33
1	0	1	0	1	1	110.00	146.67	73.33	36.67
1	0	1	1	0	0	105.00	140.00	70.00	35.00
1	0	1	1	0	1	107.00	142.67	71.33	35.67
1	0	1	1	1	0	109.00	145.33	72.67	36.33
1	0	1	1	1	1	110.00	146.67	73.33	36.67

Signal	FS4	FS3	FS2	FS1	FS0	CPU (MHz)	ZCLK (MHz)	AGP (MHz)	PCI (MHz)
0	0	0	0	0	0	100.00	133.33	66.67	33.33
0	0	0	0	0	1	100.99	134.65	67.33	33.66
0	0	0	0	1	0	103.00	137.33	68.67	34.33
0	0	0	1	0	0	100.00	133.33	66.67	33.33
0	0	0	1	0	1	103.00	137.33	68.67	34.33
0	0	1	0	0	0	100.00	133.33	66.67	33.33
0	0	1	0	1	0	103.00	137.33	68.67	34.33
0	0	1	1	0	0	100.00	133.33	66.67	33.33
0	0	1	1	0	1	103.00	137.33	68.67	34.33
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1	0	1	1	0	0	105.00	140.00	70.00	35.00
1	0	1	1	0	1	107.00	142.67	71.33	35.67
1	0	1	1	1	0	109.00	145.33	72.67	36.33
1	0	1	1	1	1	110.00	146.67	73.33	36.67

QUANTA
COMPUTER

Title

CLK GEN & DRAM Buffer

Size

Document Number

Rev

AW1 M/B

1B

Date:

Thursday, August 12, 2004

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of

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03

VCC3

C1 0.1U

FBM2125HM330

C9 10U/10V/Y5U

C2 0.1U

C3 0.1U

C4 0.1U

C5 0.1U

C6 0.1U

C7 0.1U

C8 0.1U

C1065 0.1U

VCC3

R14 10K

R16 10K

Q2 MMBT3904

Q1 MMBT3904

VCORE

R24 10K

VCC3

R27 10K

FS0

R28 *10K

R29 10K

FS1

R30 *10K

R31 10K

FS2

R32 *10K

R33 *10K

FS3

R34 10K

R35 *10K

FS4

R36 10K

4.5 CPUPWRGD_CPU

R1053

0 PD#

R19 475/F

IREF

4.21,41 -CPUSTOP

-CPUSTOP 4

VCC3

L2 MLB_160808-0300P-N2

300 ohms@100MHz

C18 0.1U

C19 4.7U

GND

Y1

14.318MHz/20PF/30ppm

C27 27P

C28 27P

VCC3

R37 *10K

Q3 *2N7002E

R962 0

10,21 SMBCLK

CGCLK SMB

U1 ICS952018

VDDREF

VDD2

VDDPCI

VDDPCI

VDD48

VDDAGP

VDDCPU

VDDSRC

GNDREF

GND2

GNDPCI

GNDPCI

GND48

GNDAGP

GNDCPU

GNDSRC

CLK VDD1

11

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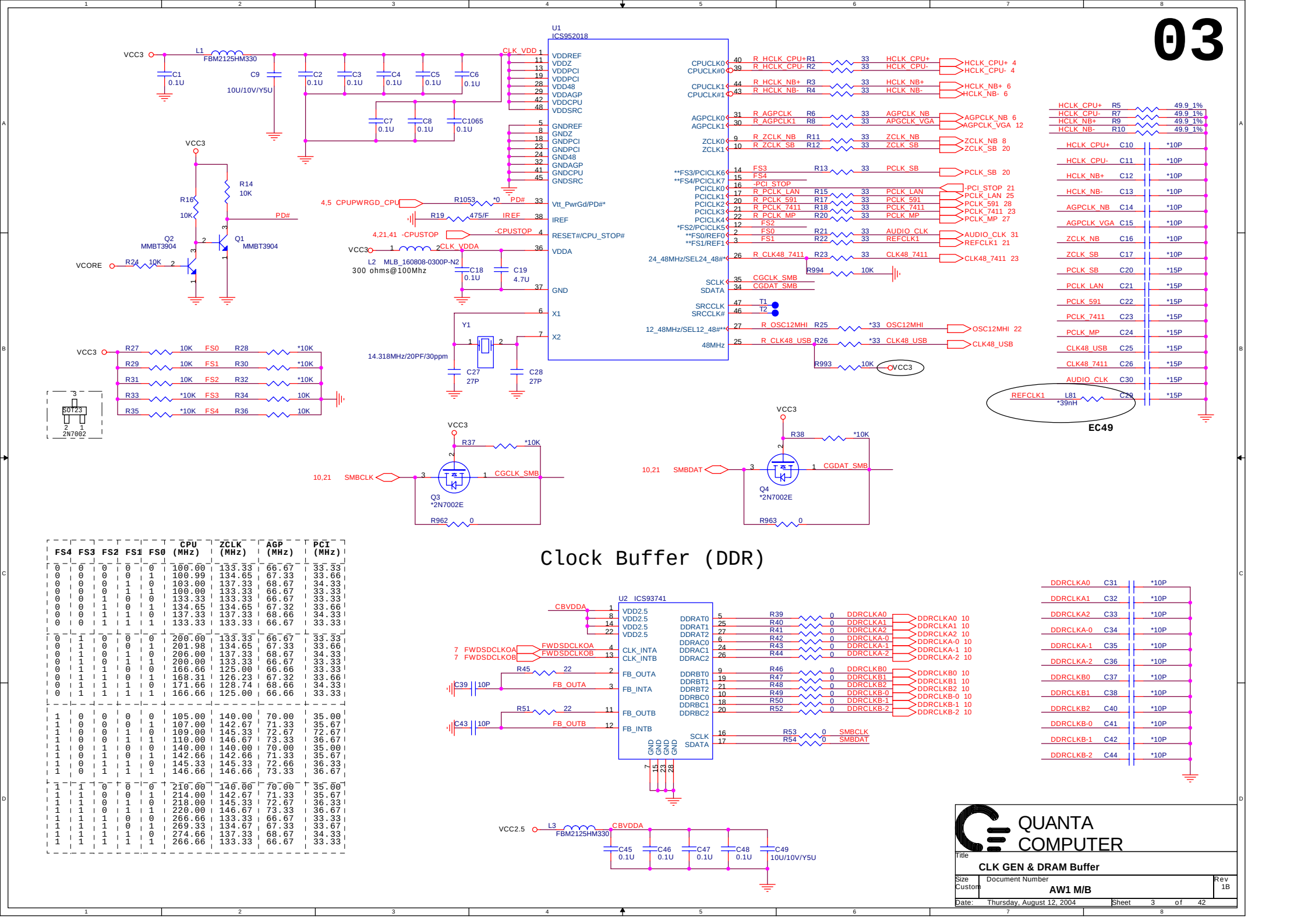
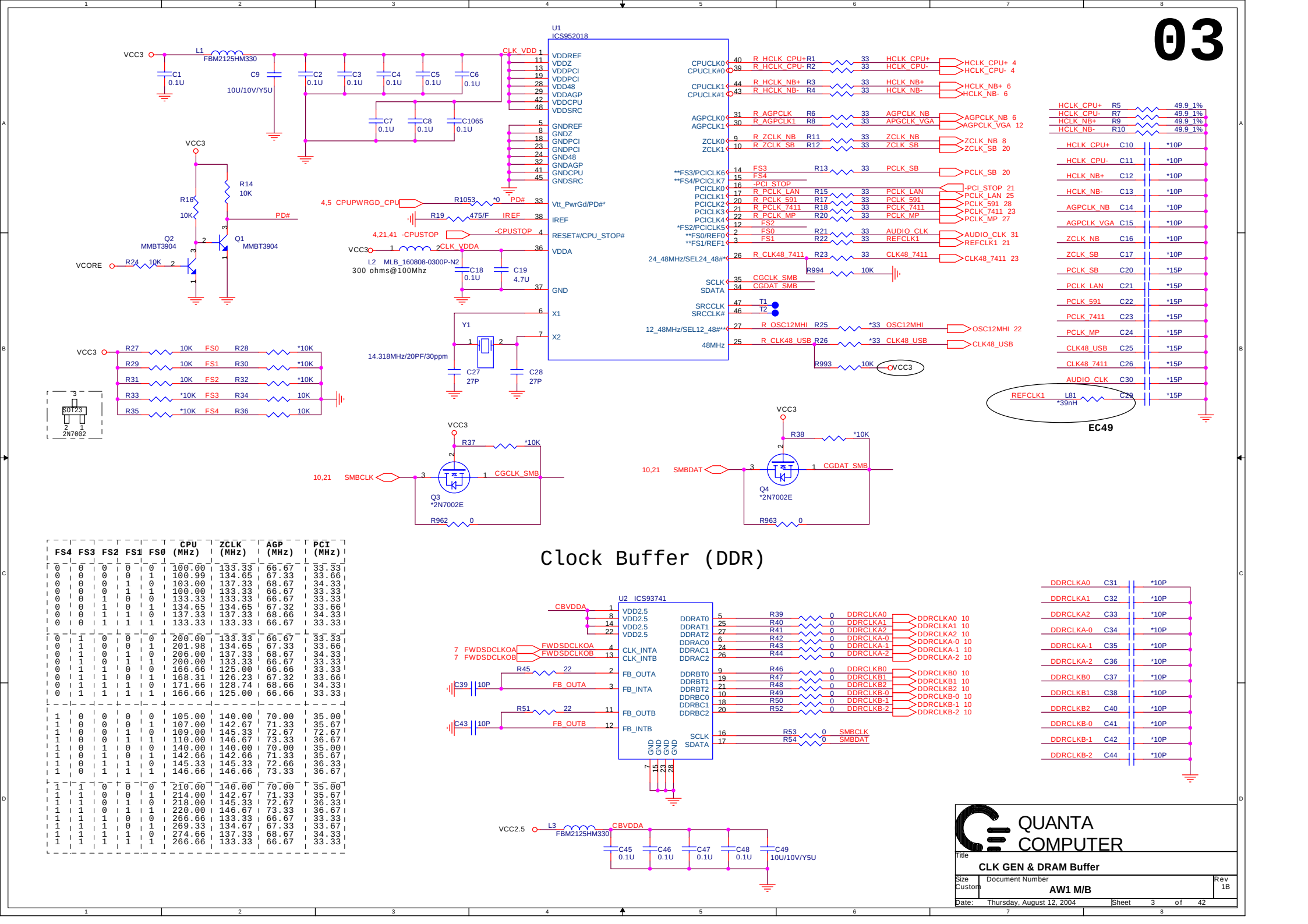
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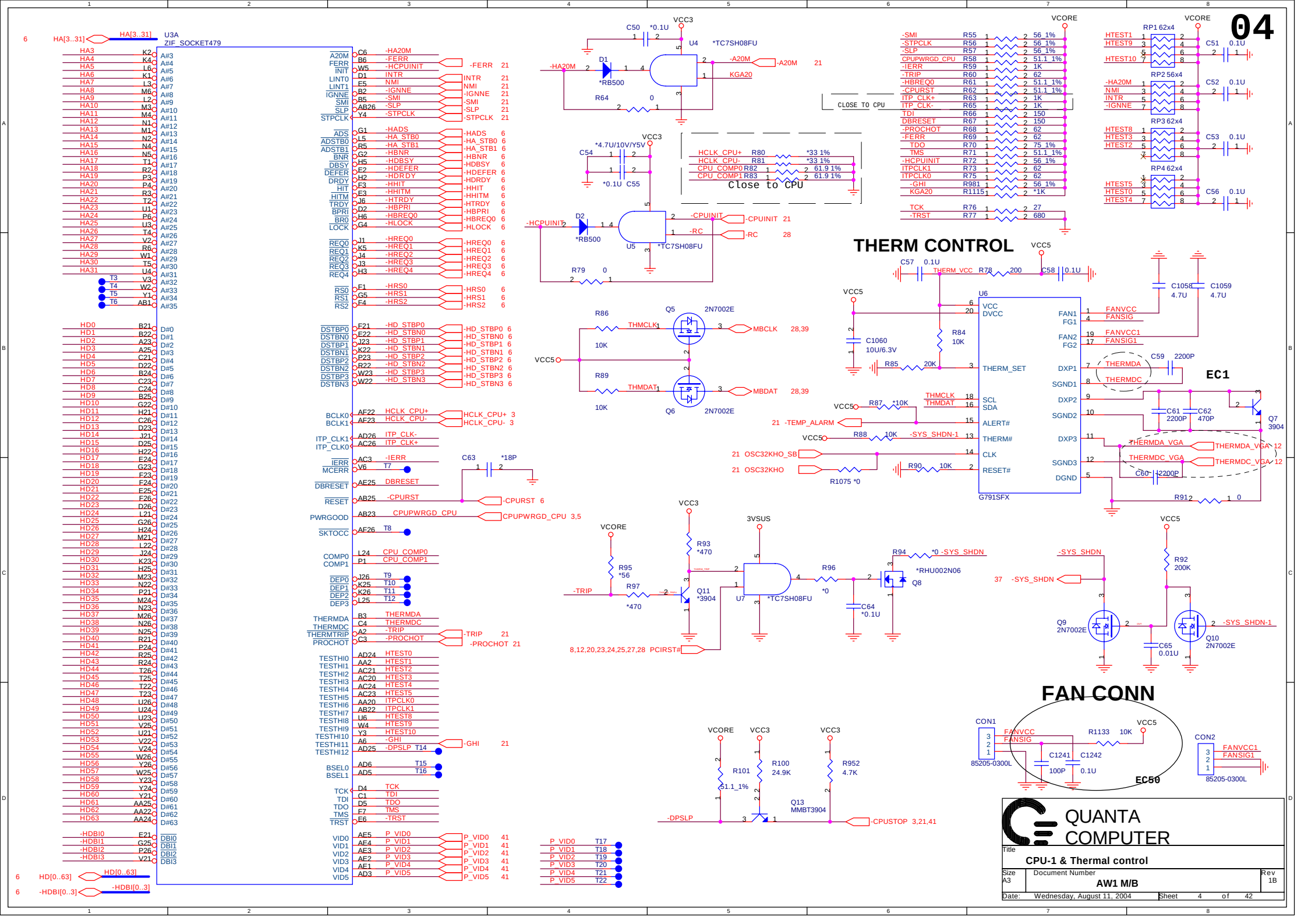
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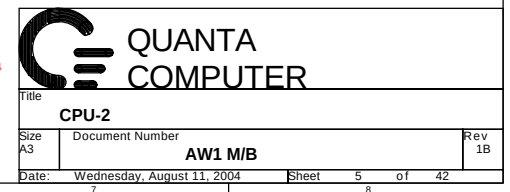
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06

AGP

HOST

655FX_6

QUANTA COMPUTER

NB(655FX HOST & AGP)

File: NB(655FX HOST & AGP)
 Size: A3
 Document Number: AW1 M/B
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06

AGP

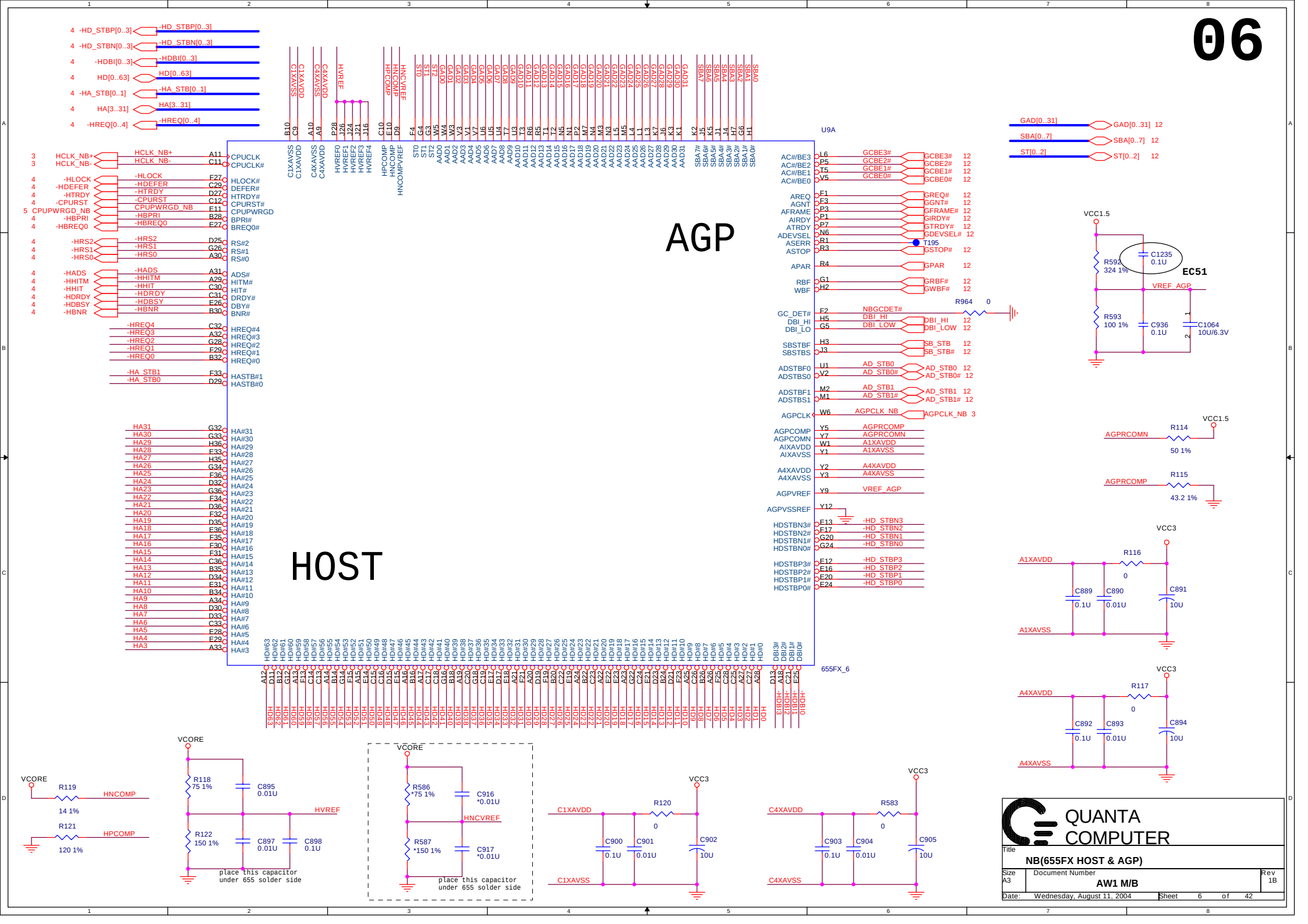
HOST

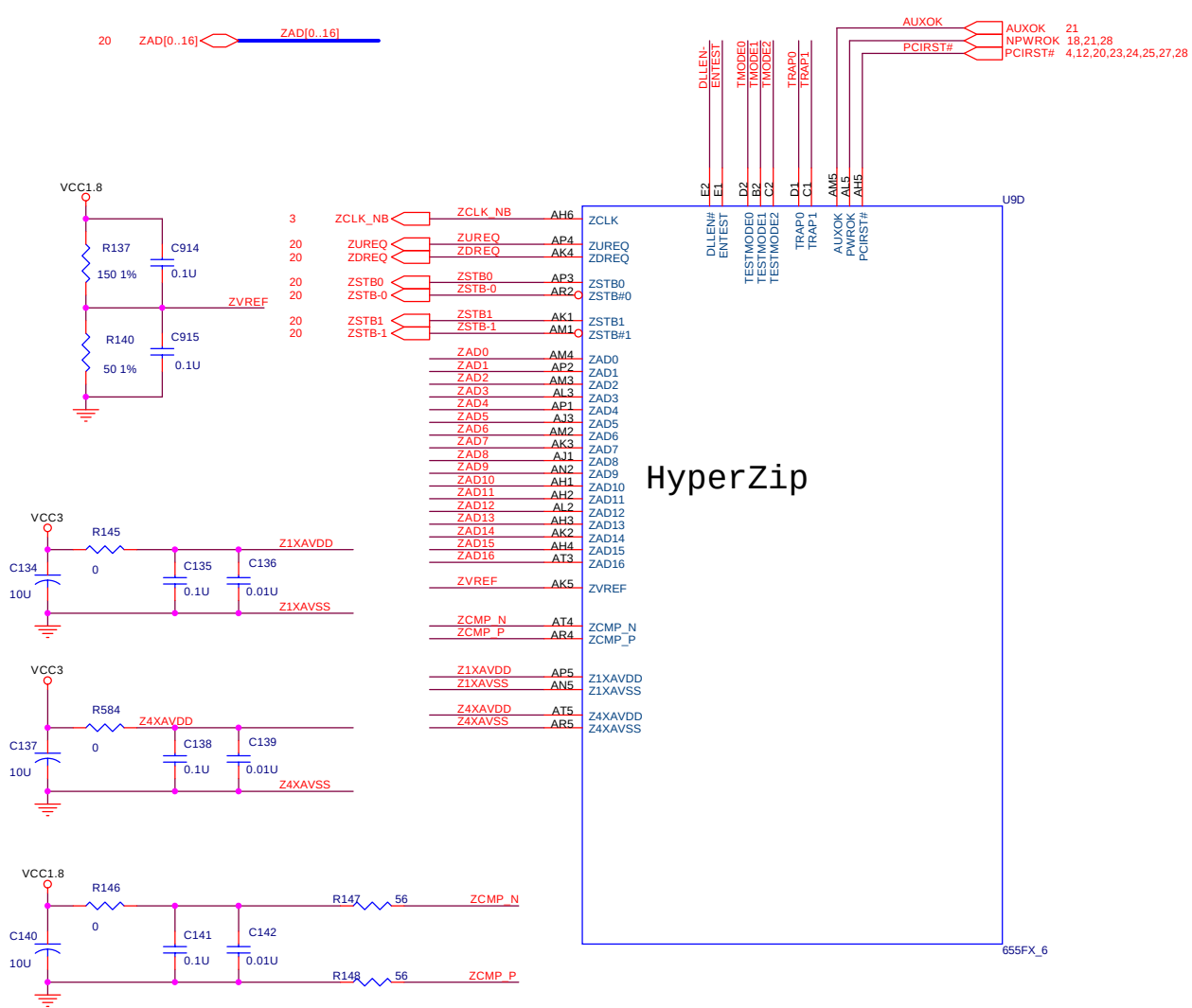
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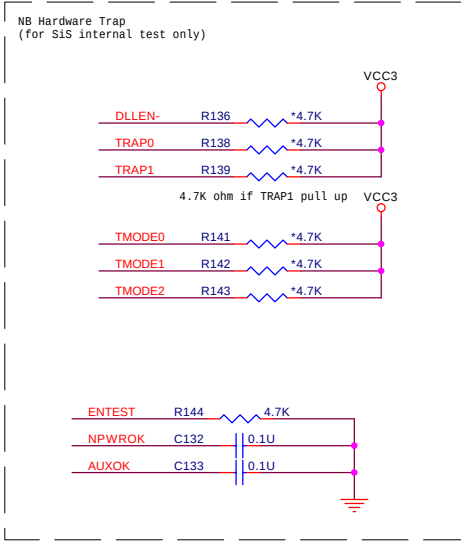
NB(655FX HOST & AGP)

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 Size: A3
 Document Number: AW1 M/B
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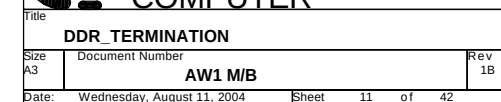
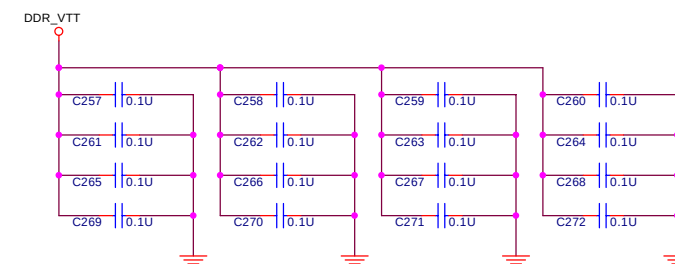
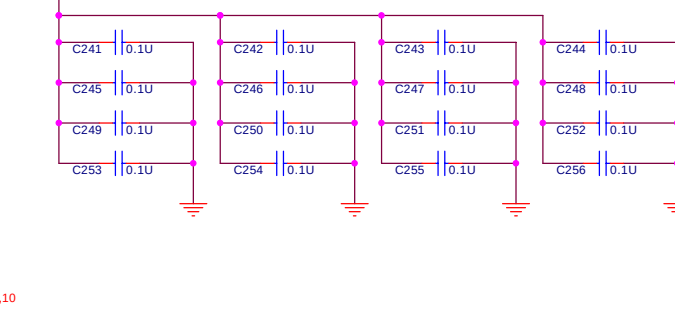
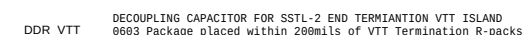


HyperZip









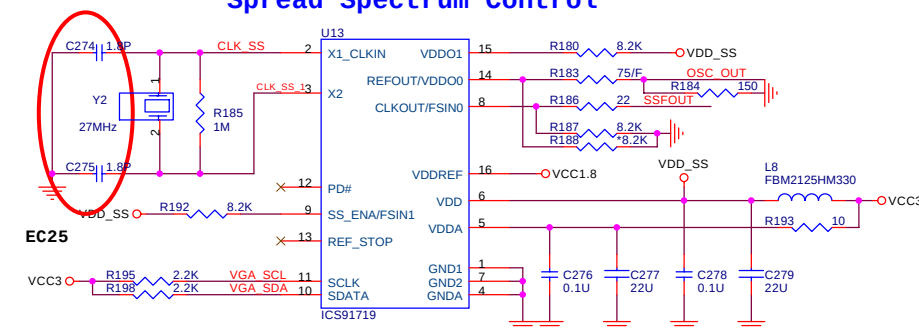
Strapping

VMEM 64/128 MB no stuff

GPI01	GPI00	AGP 1X CLOCK FEEDBACK PHASE ADJUST WITH RESPECT TO REFCLK
L0	L0	REFCLK SLIGHTLY EARLIER THAN FEEDBACK (DEFAULT)

GPI03	GPI02	CLOCK PHASE ADJUSTMENT BETWEEN X1 AND X2 CLK
L0	L0	0 TAP DELAY (DEFAULT)

Spread Spectrum Control



INPUT SELECT FUNCTIONALITY

PIN14	PIN15	REF VOLTAGE
0	1	1.8V

REF VOLTAGE SELECT FUNCTIONALITY

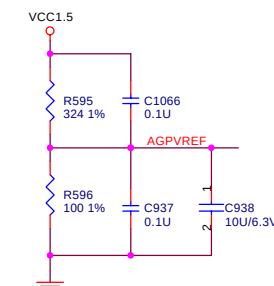
FS_IN1	FS_IN0	MHZ
1	0	27.00 IN/OUT

LOCATION	R953, R954, R955, R956, R957, R958, R959 U23, C522, R304, R307, R310, R311, R312
VRAM SIZE	
32/64/128	CANCEL
256	MOUNT

HDTV_SETECT-1(ZV_LCDDATA7)

L: S-Video

H: HDTV



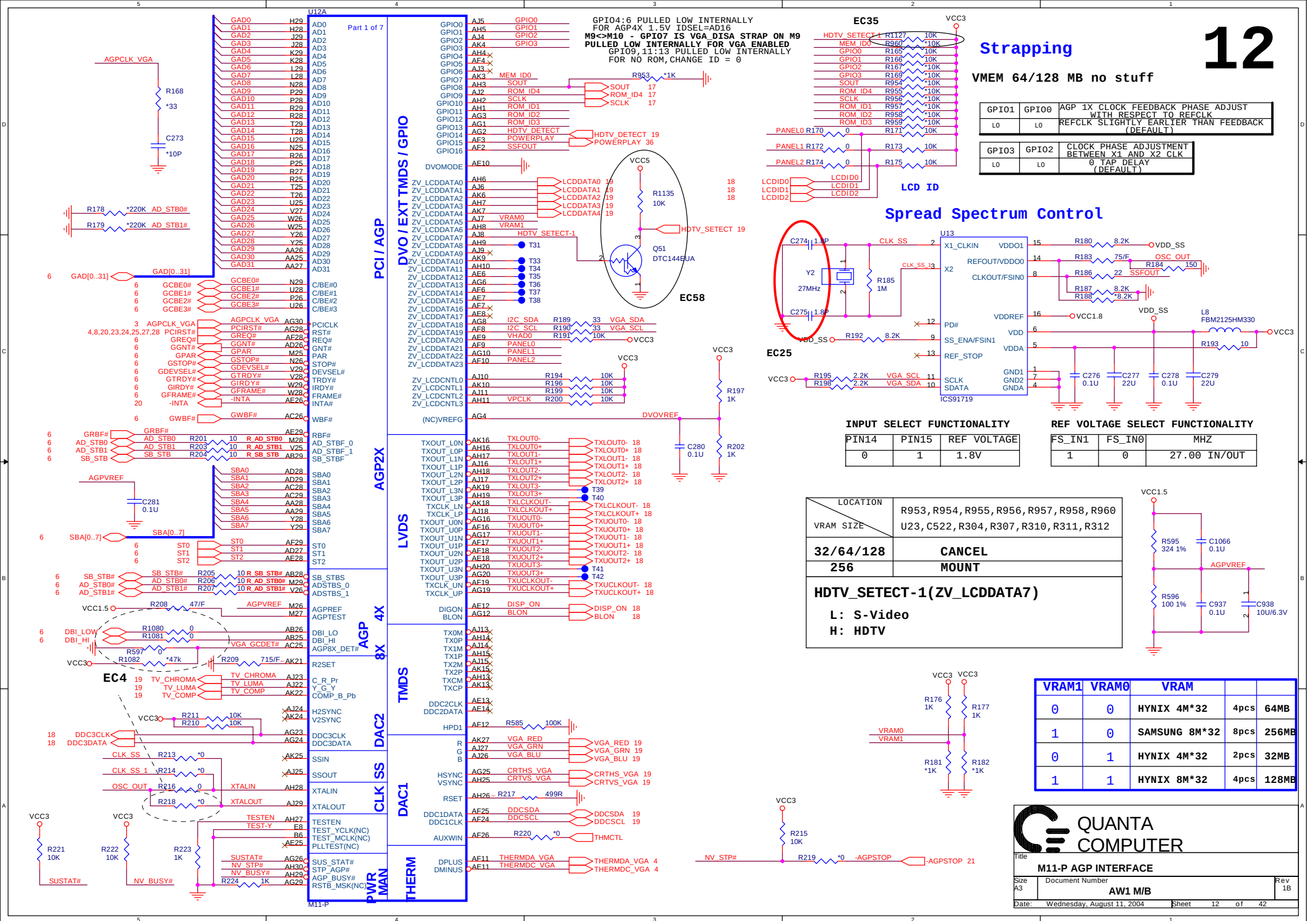
VRAM1	VRAM0	VRAM		
0	0	HYNIX 4M*32	4pcs	64MB
1	0	SAMSUNG 8M*32	8pcs	256MB
0	1	HYNIX 4M*32	2pcs	32MB
1	1	HYNIX 8M*32	4pcs	128MB



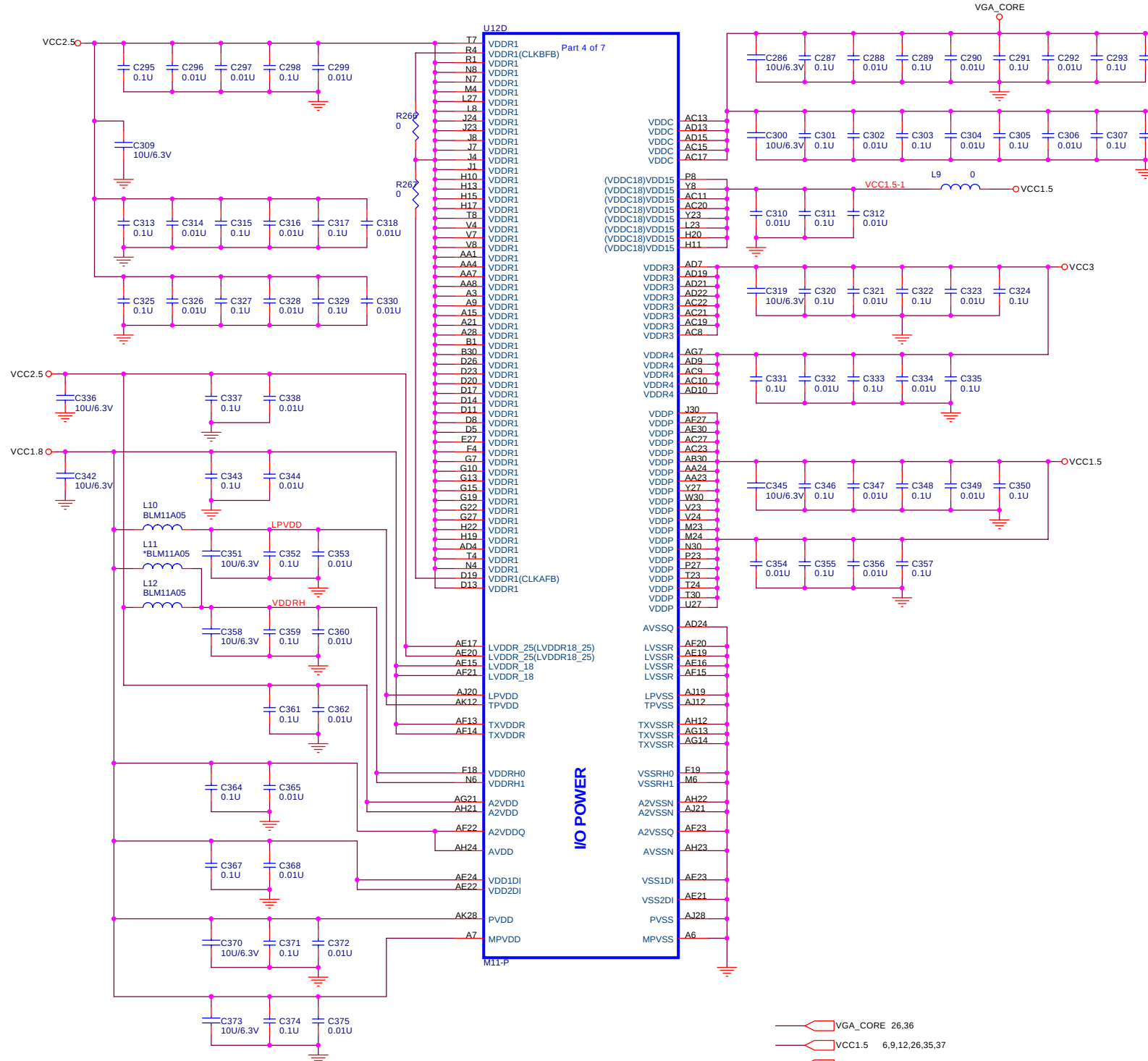
QUANTA
COMPUTER

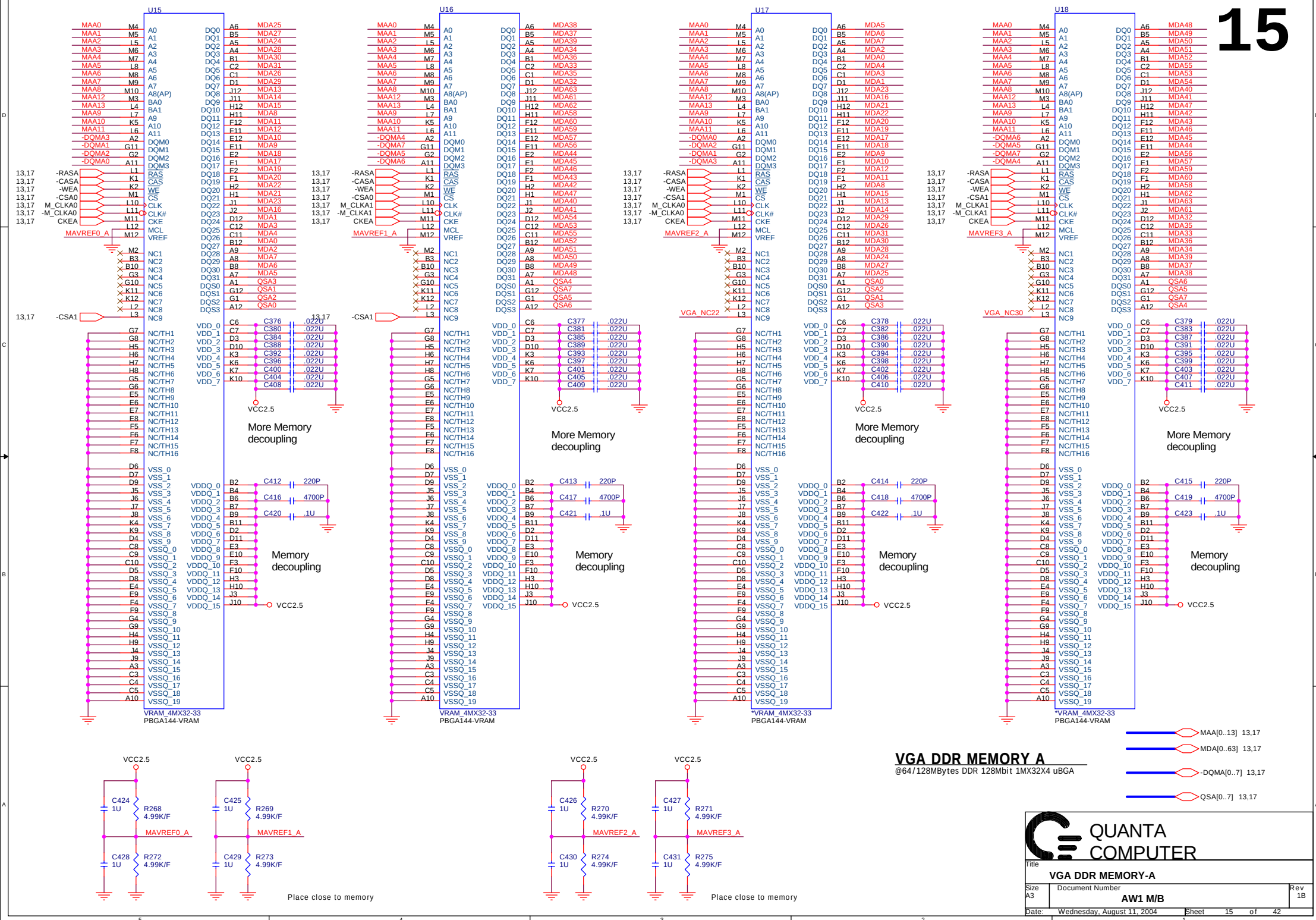
M11-P AGP INTERFACE

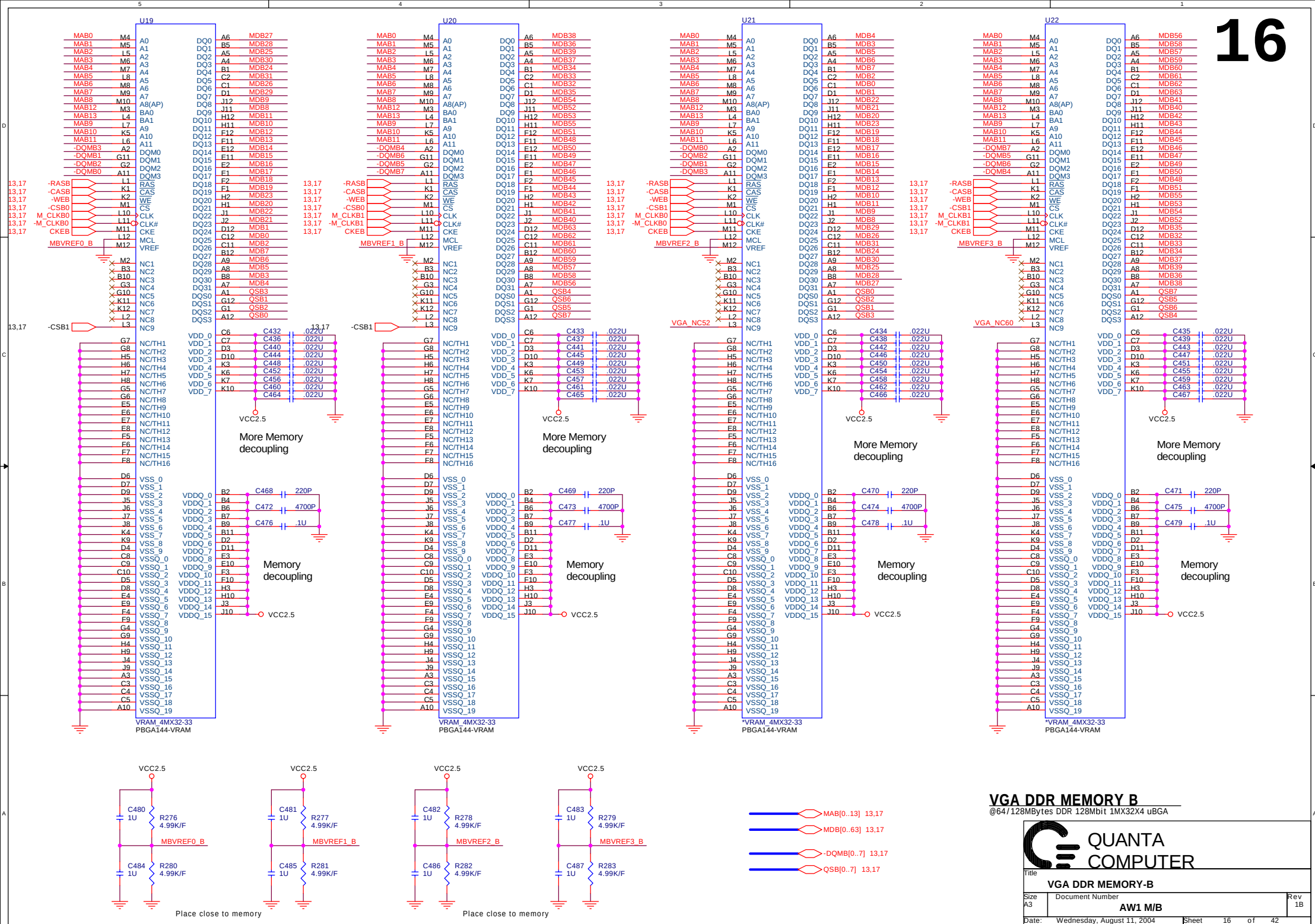
Size A3	Document Number AW1 M/B	Rev 1E
Date	Wednesday, August 11, 2004	Sheet 12 of 42

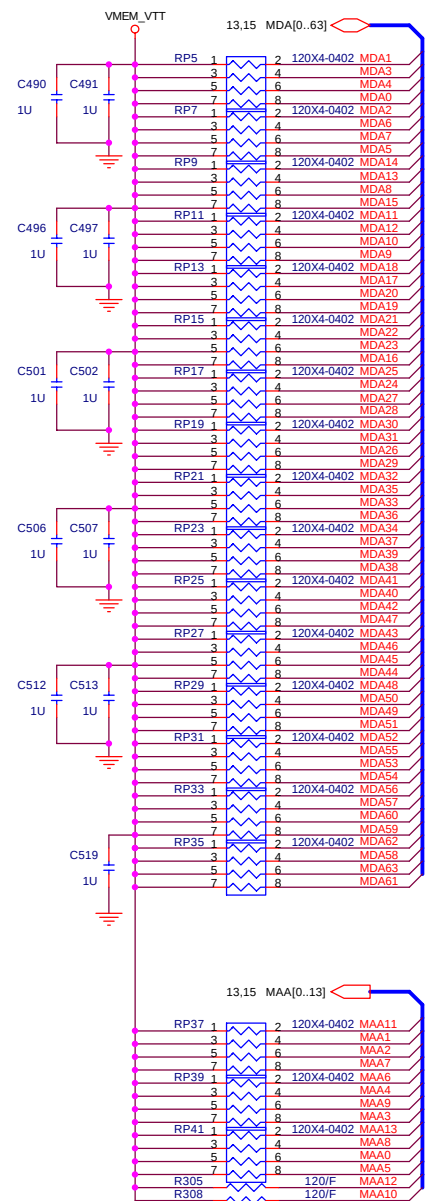




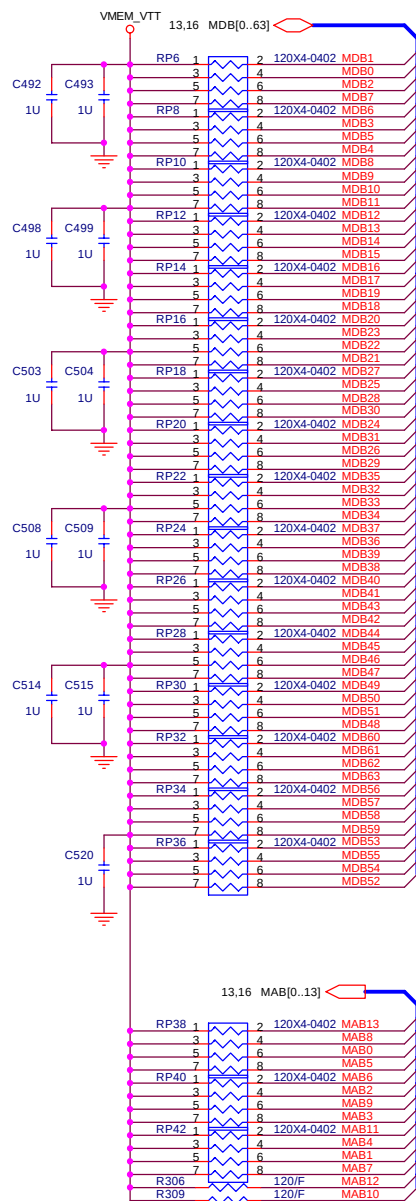




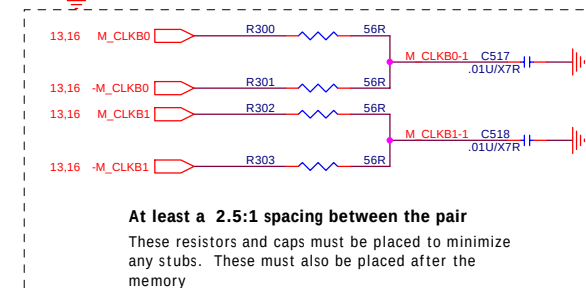
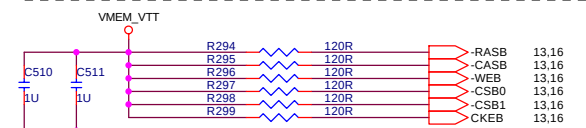
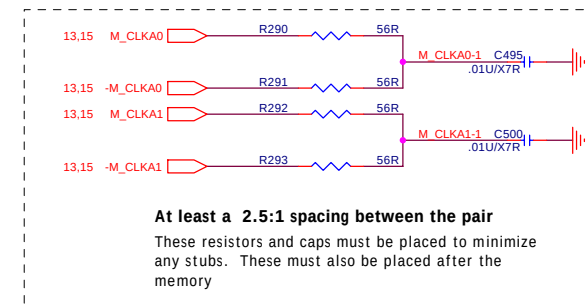
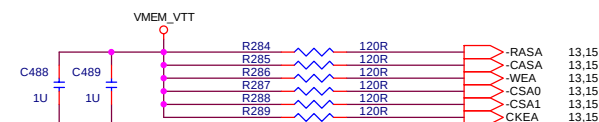
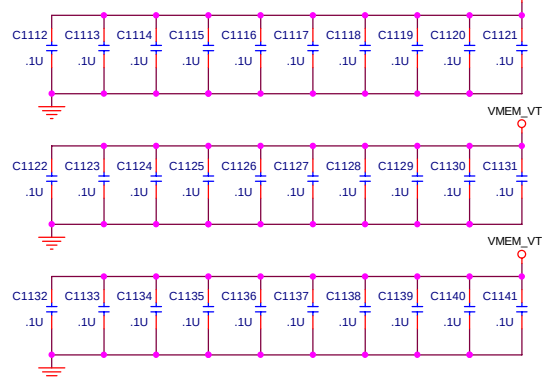
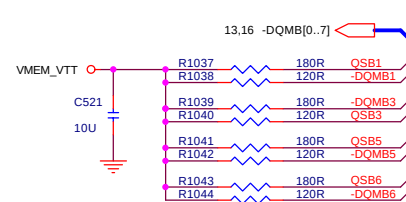
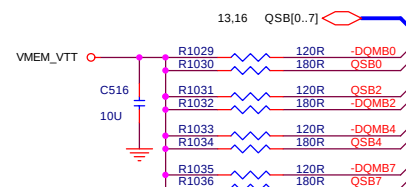
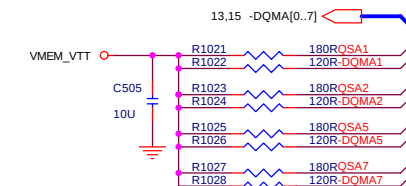
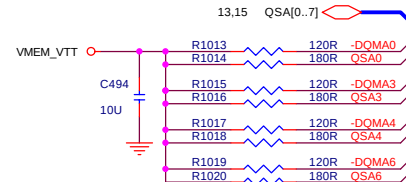




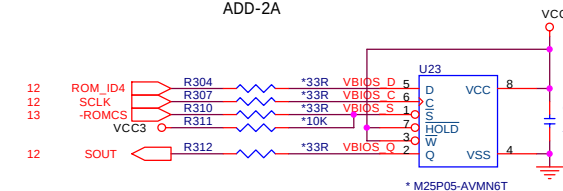
Place at nets mid point



Place at nets mid point

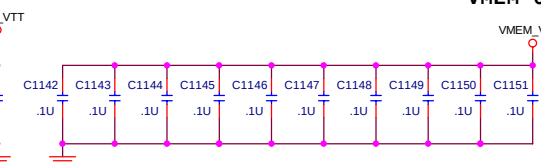
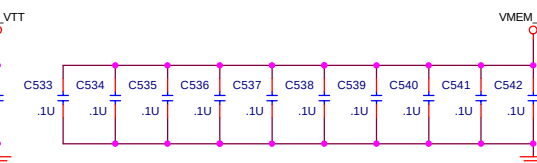
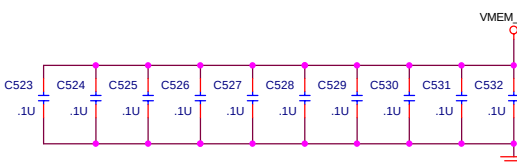


ADD-2A



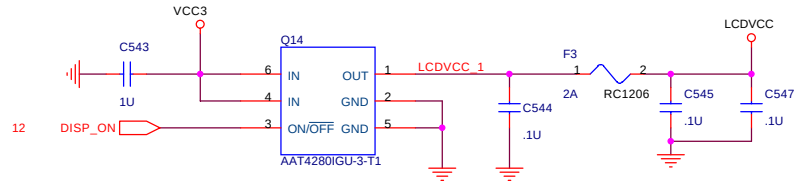
VMEM 64/128 MB no stuff

SERIAL ROM

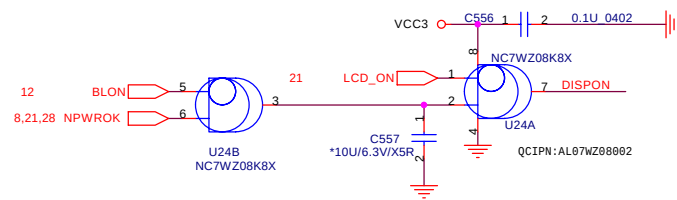


Title	
DDR VRAM PULL UP	
Size	Document Number
Custom	AW1 M/B
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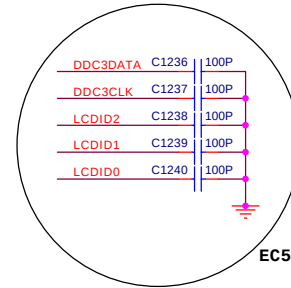
PANEL VCC CONTROL



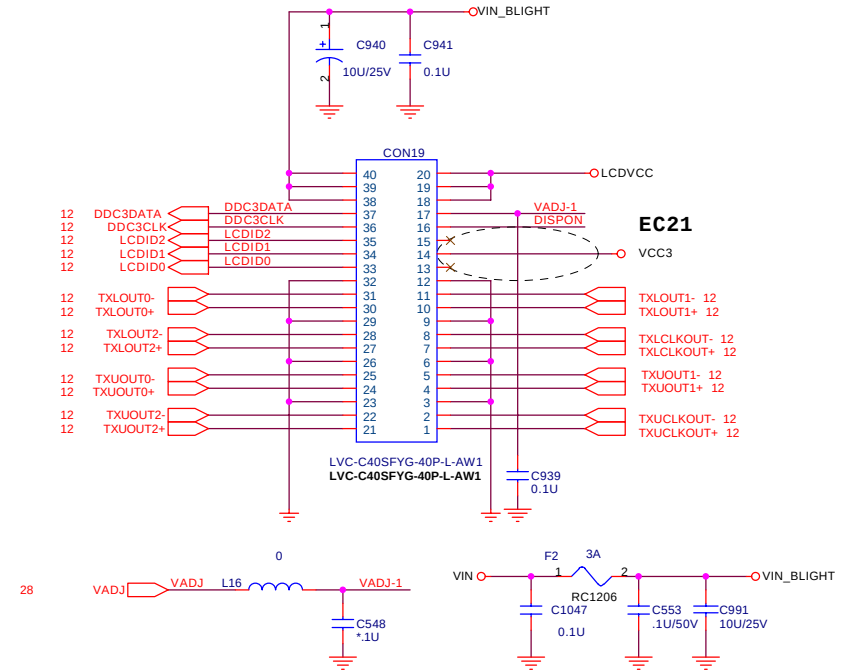
BACKLIGHT CONTROL



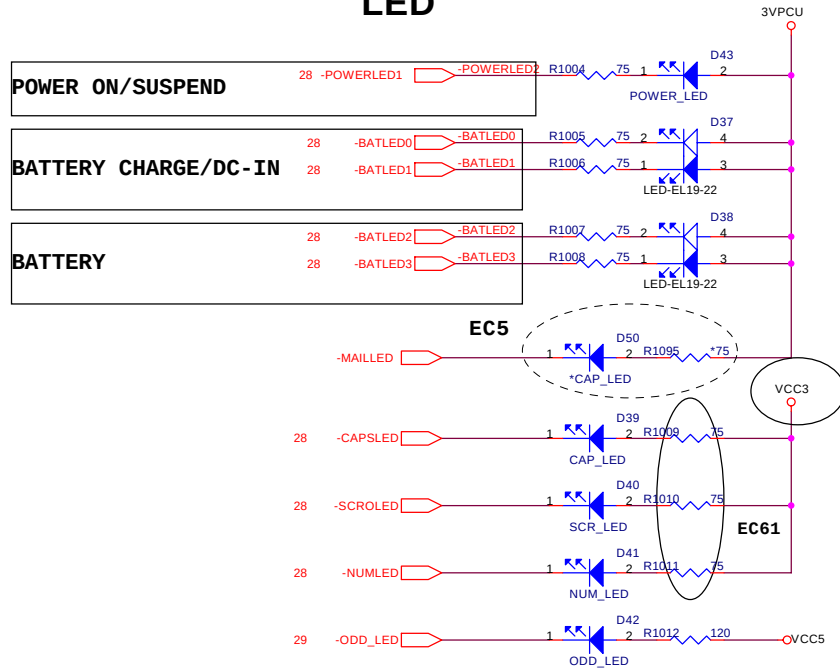
LCD CONNECTOR



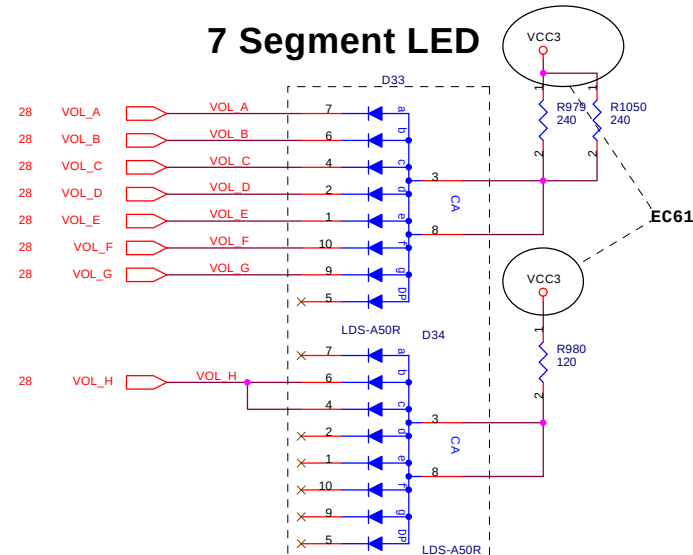
EC52



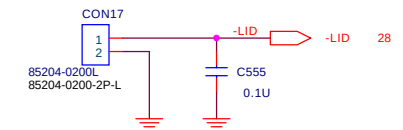
LED



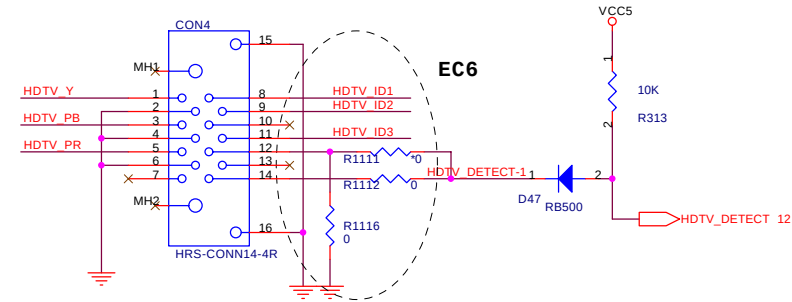
7 Segment LED



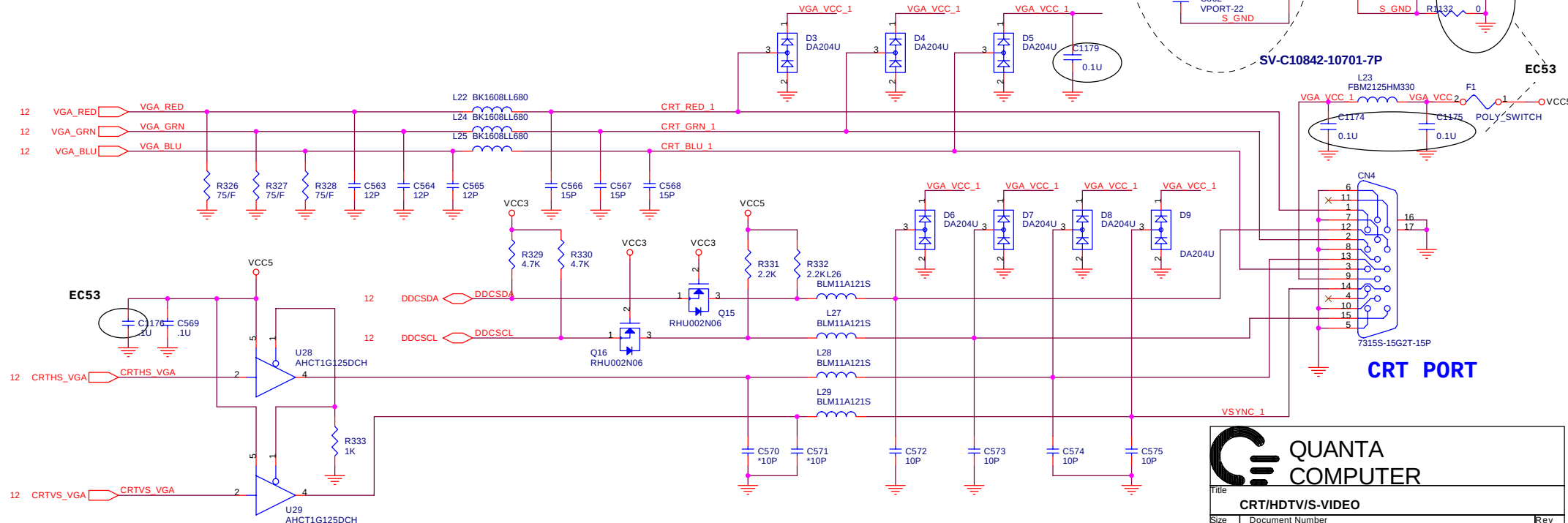
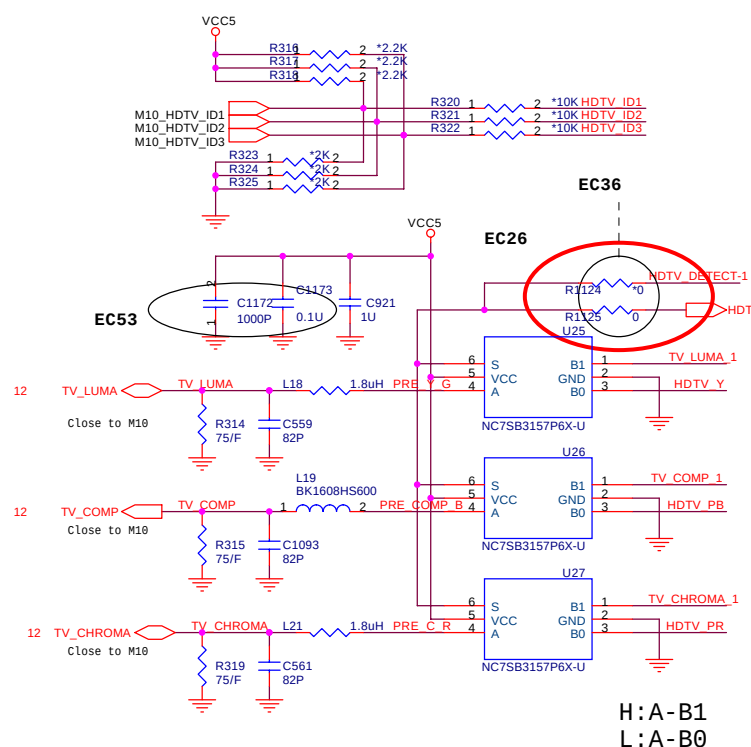
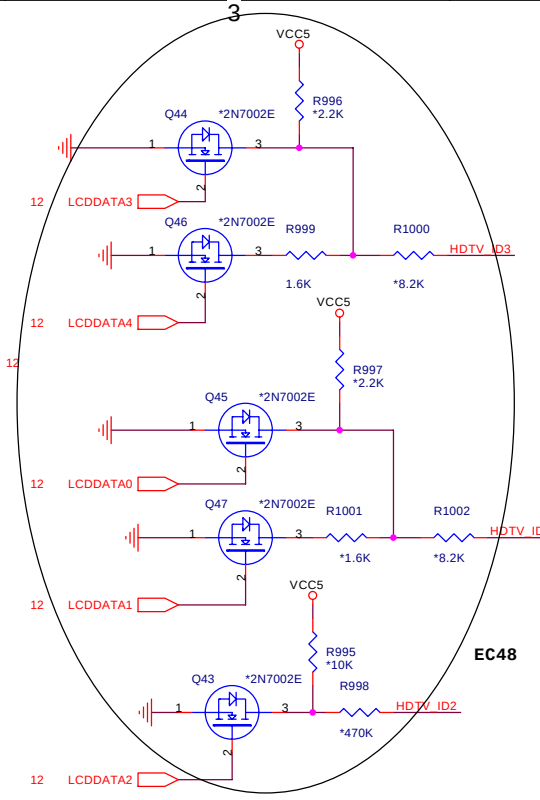
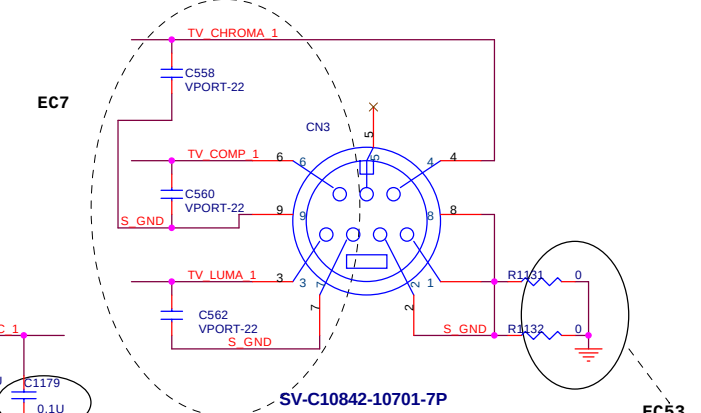
LID

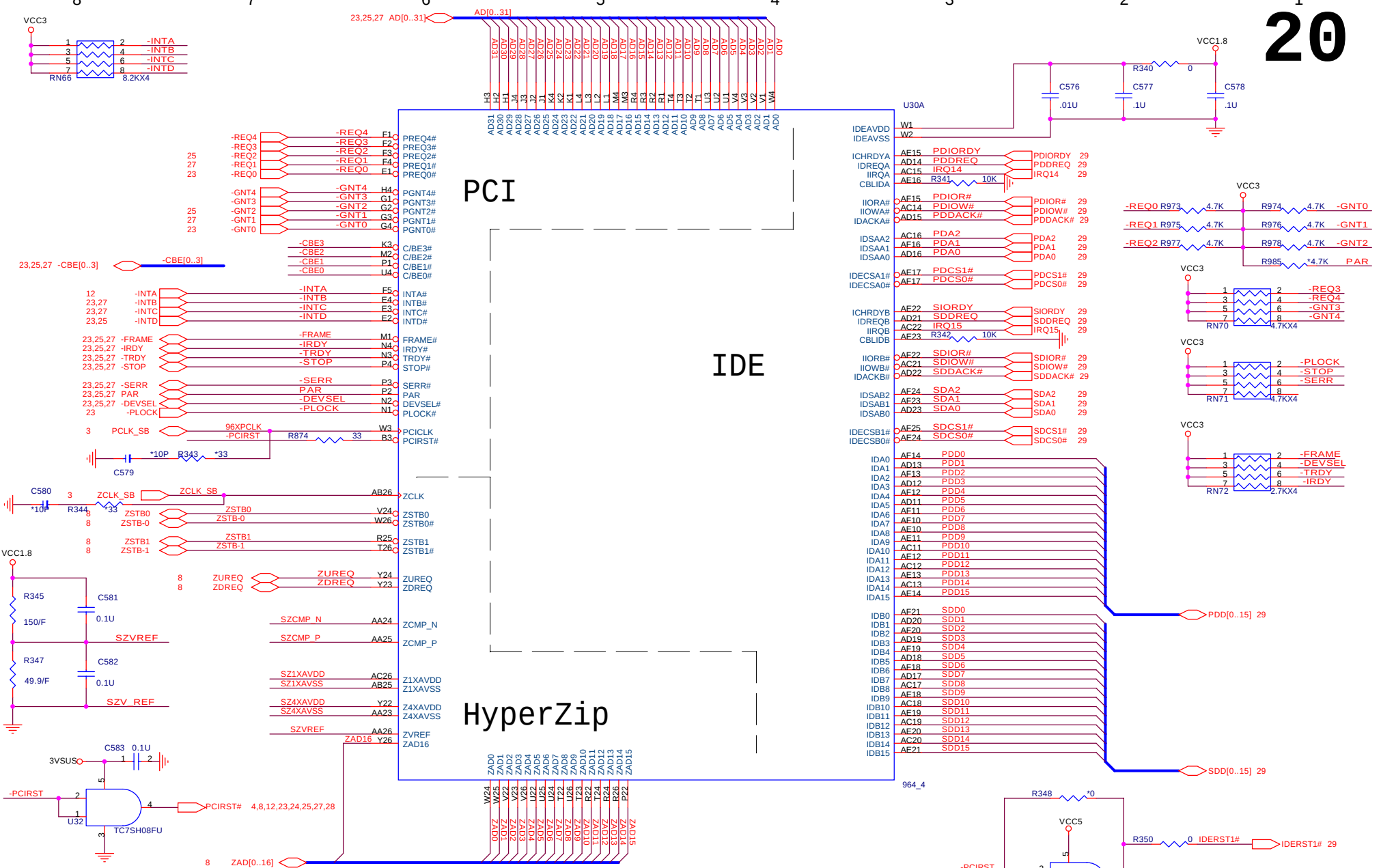


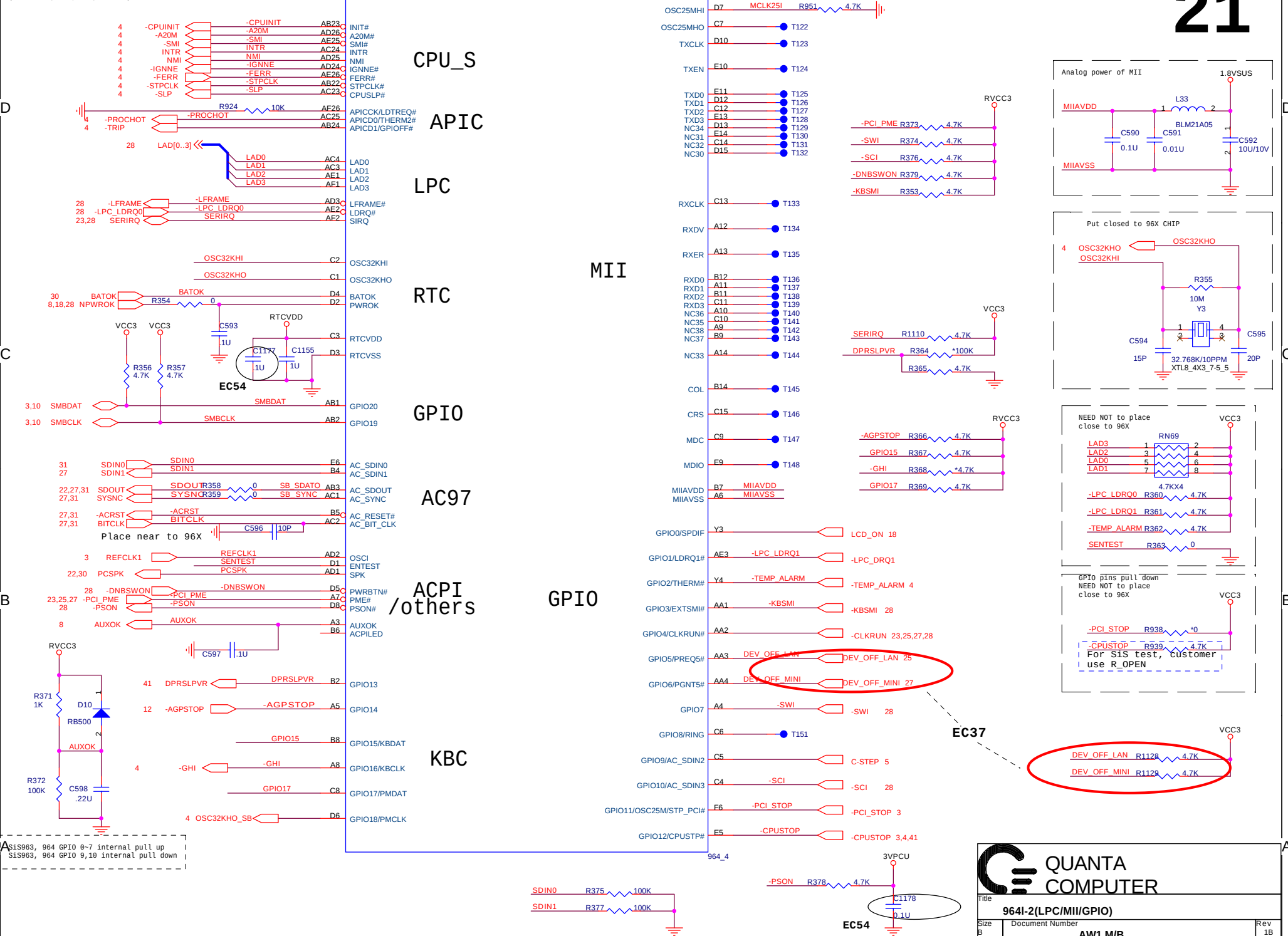
HDTV

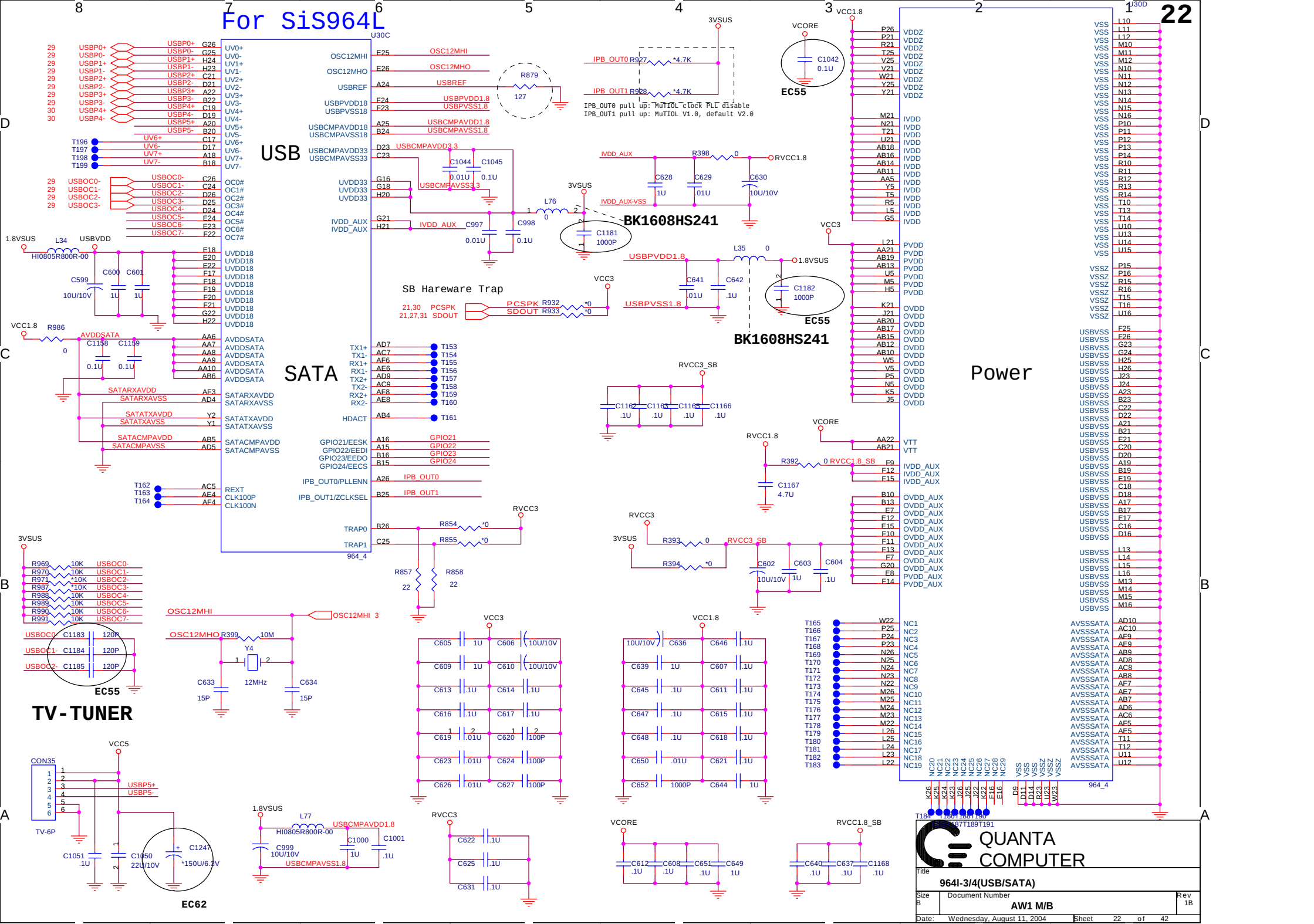


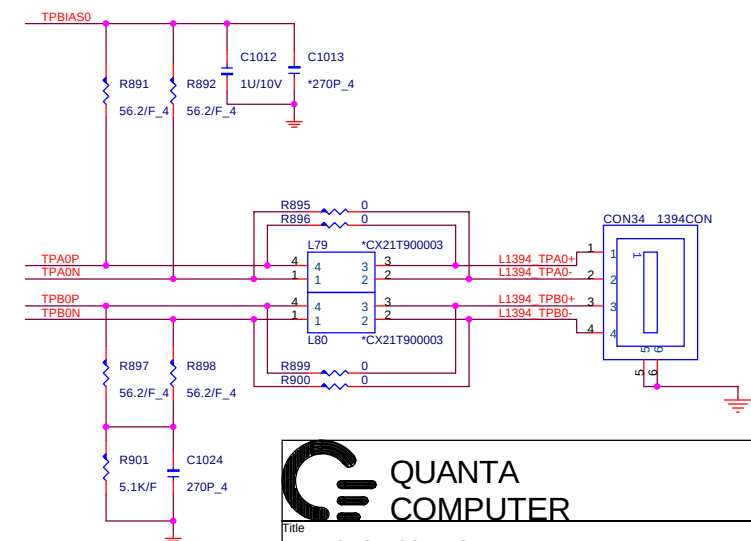
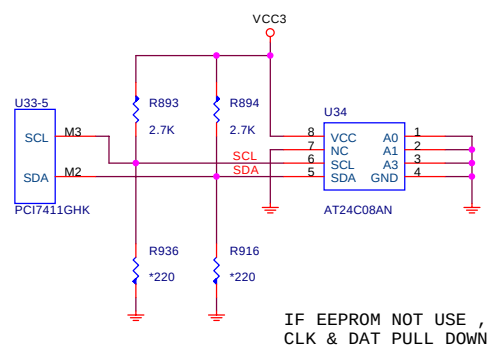
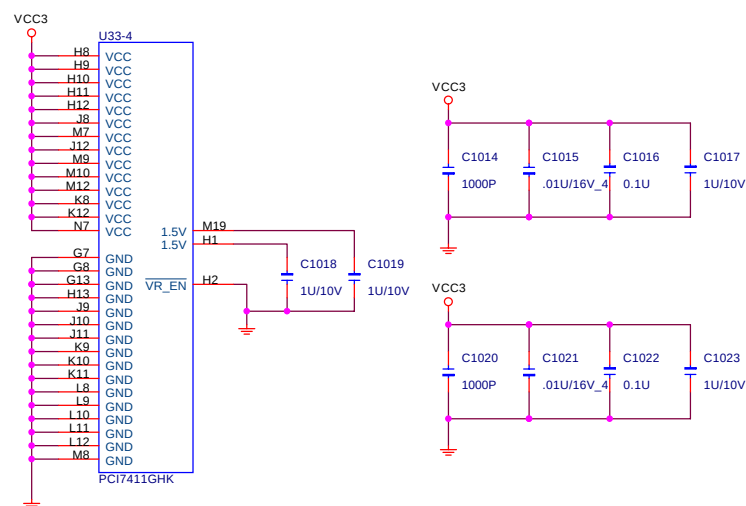
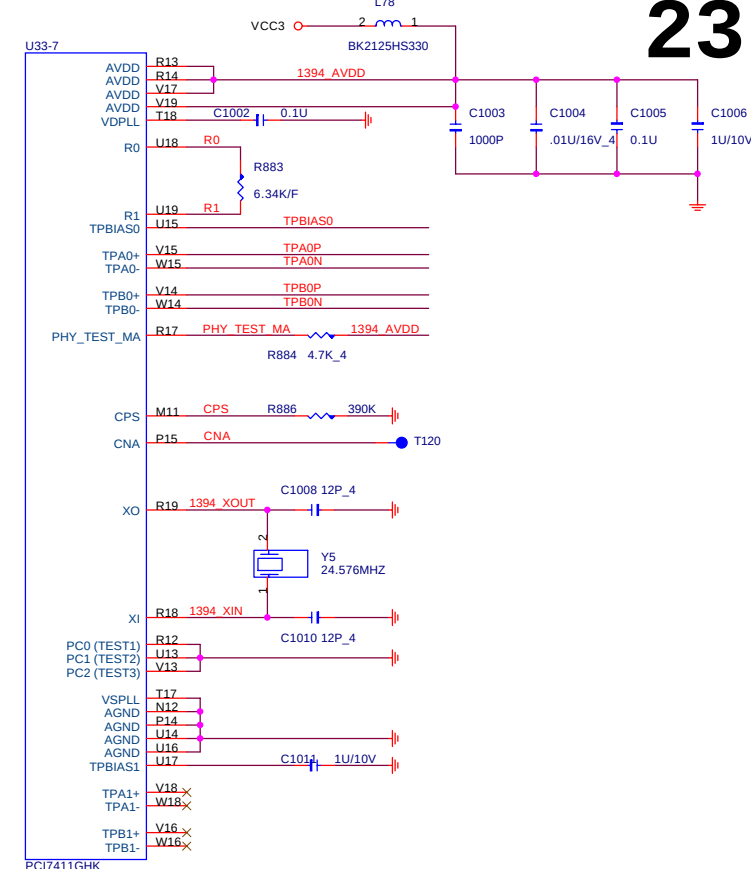
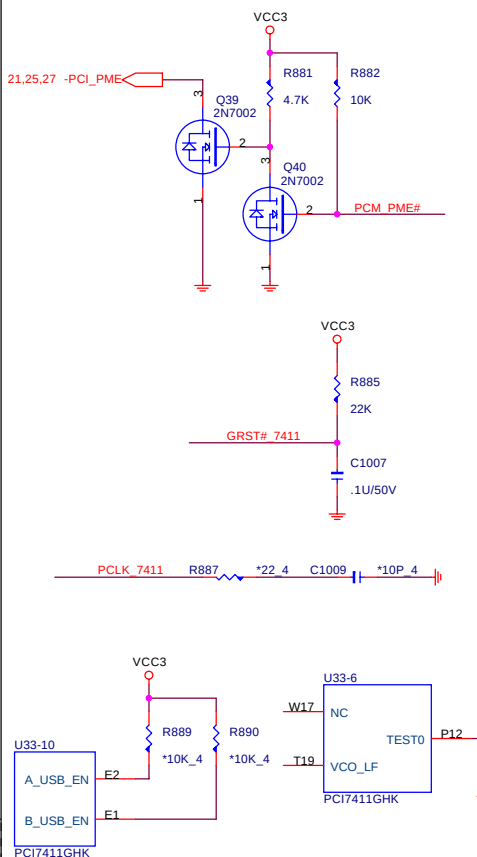
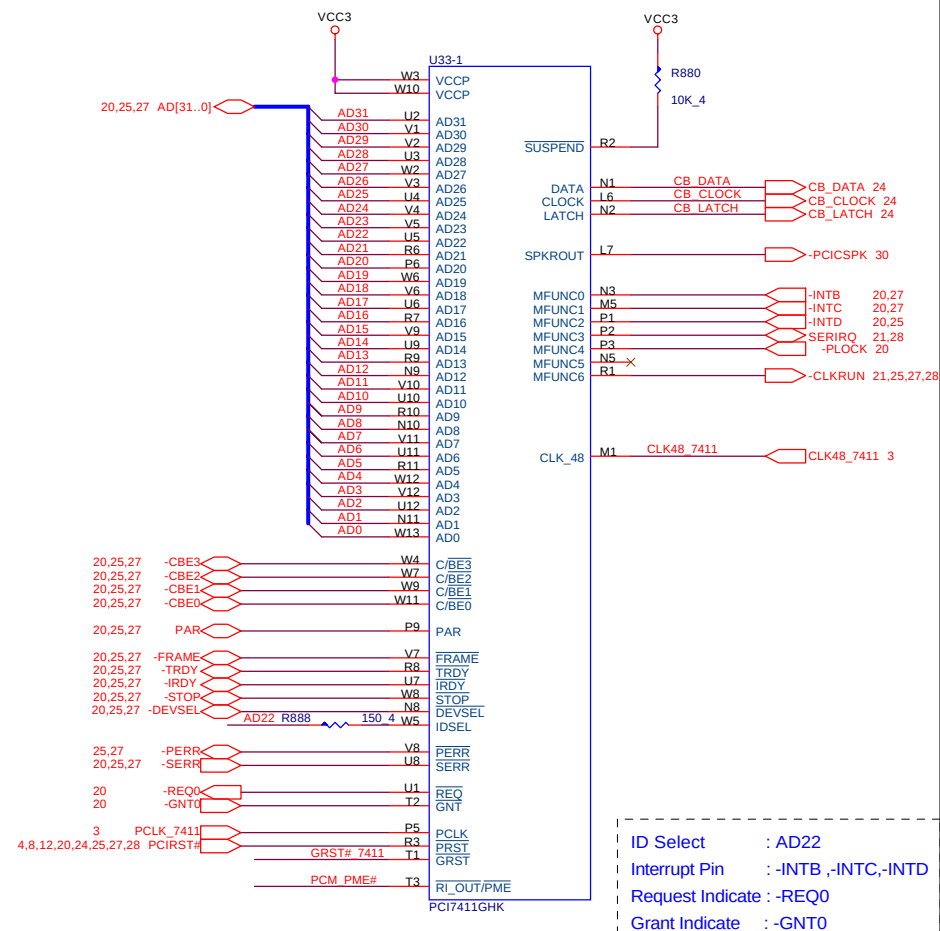
S-VIDEO

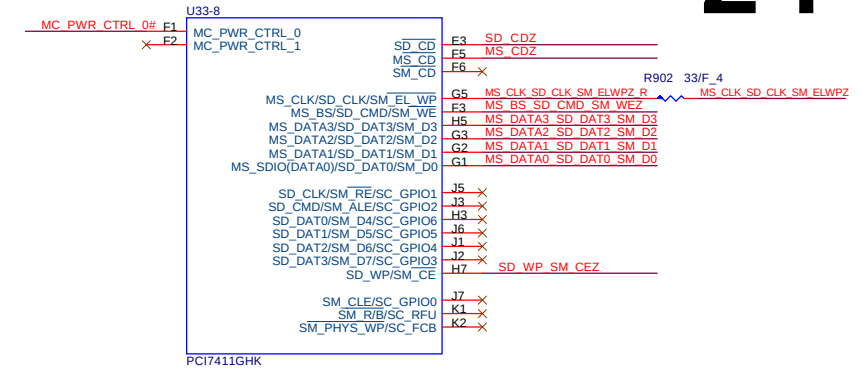
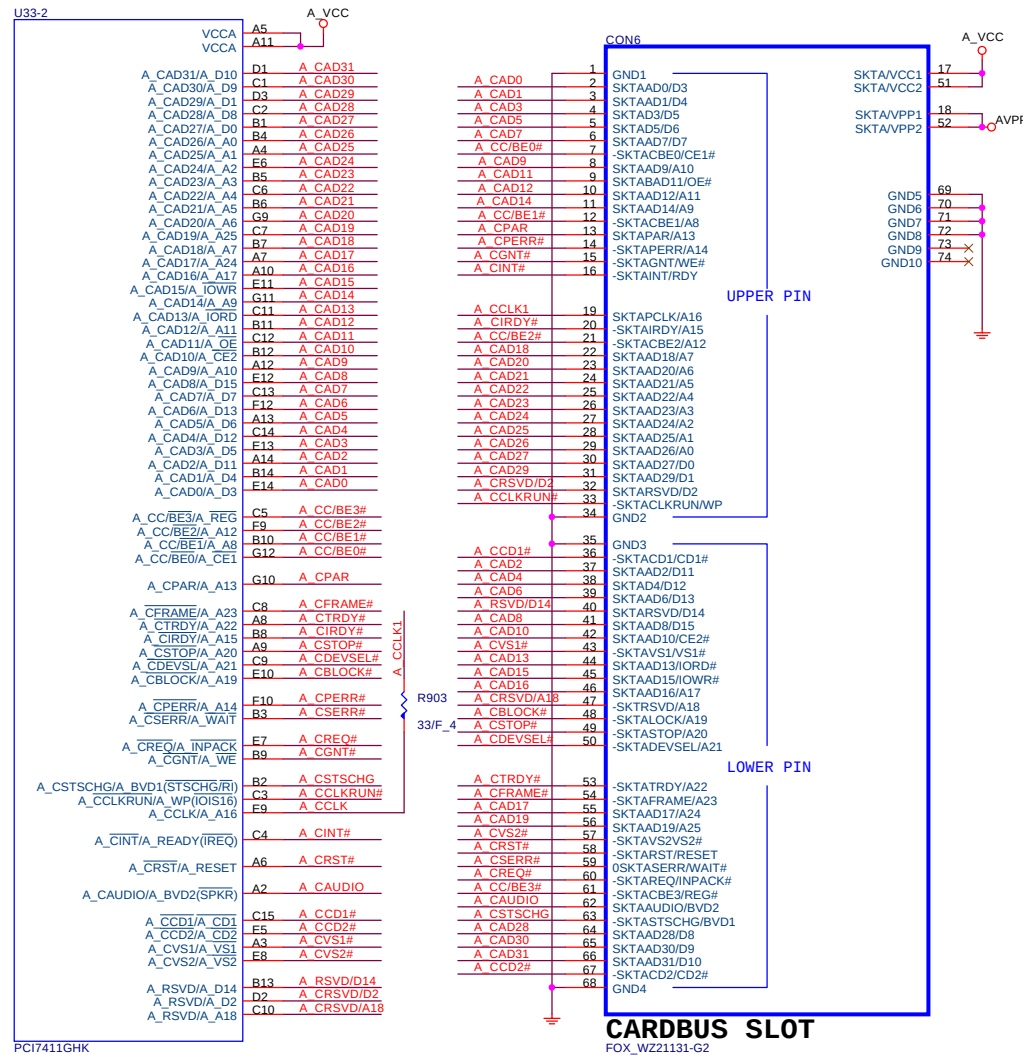




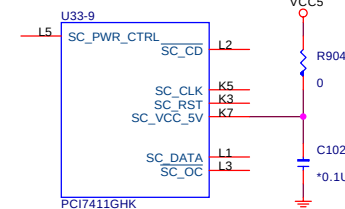
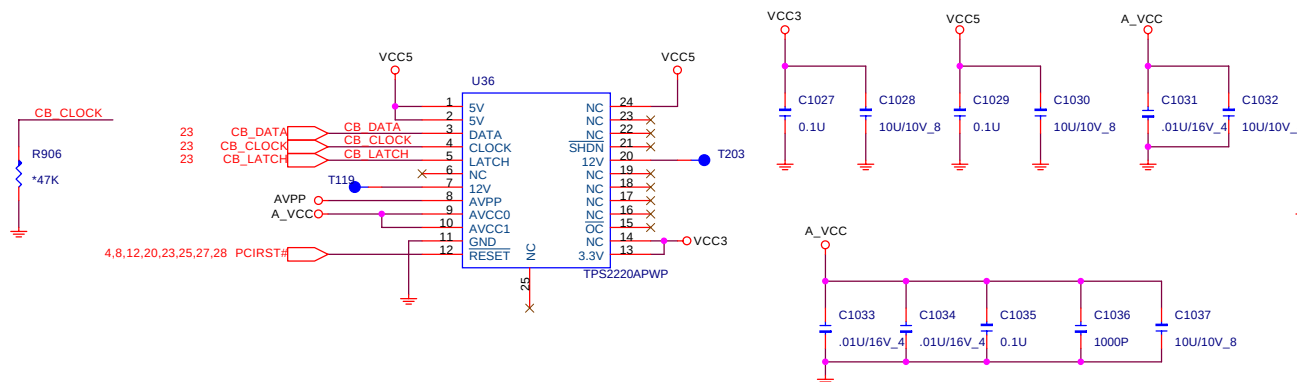
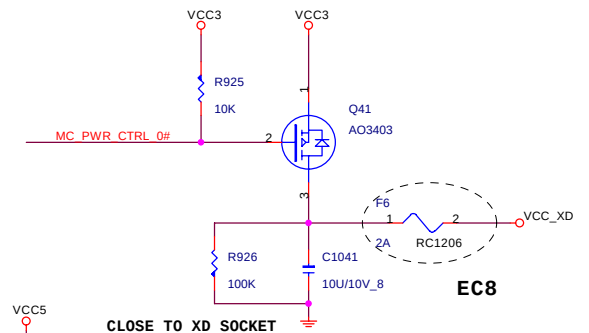
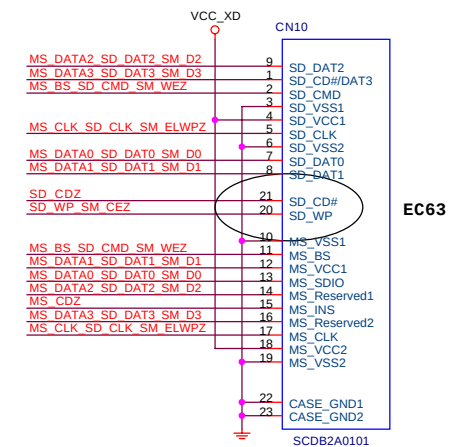








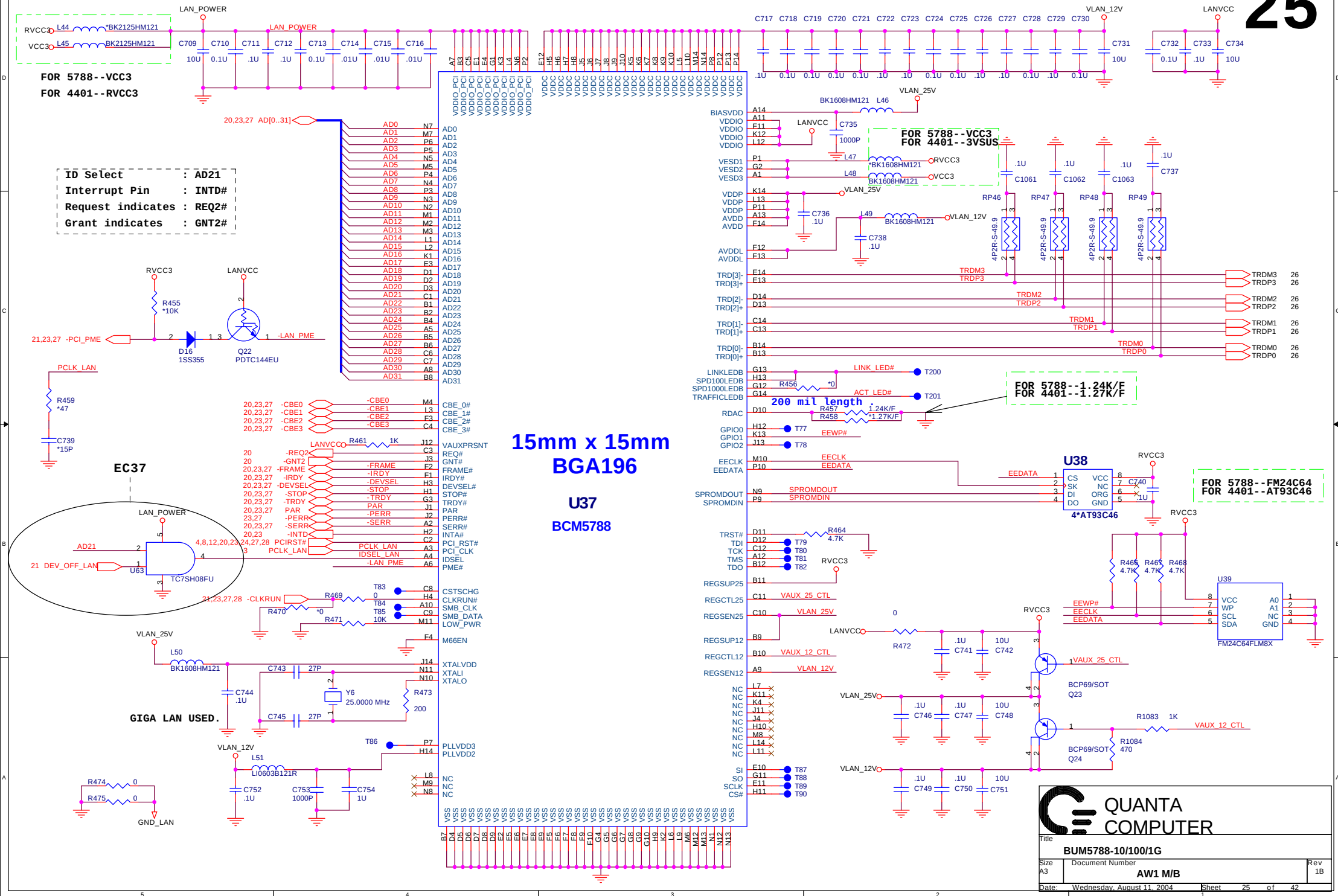
3 IN 1 CARD READER



BCM4401- -10/100
BCM5788- -10/100/GIGA

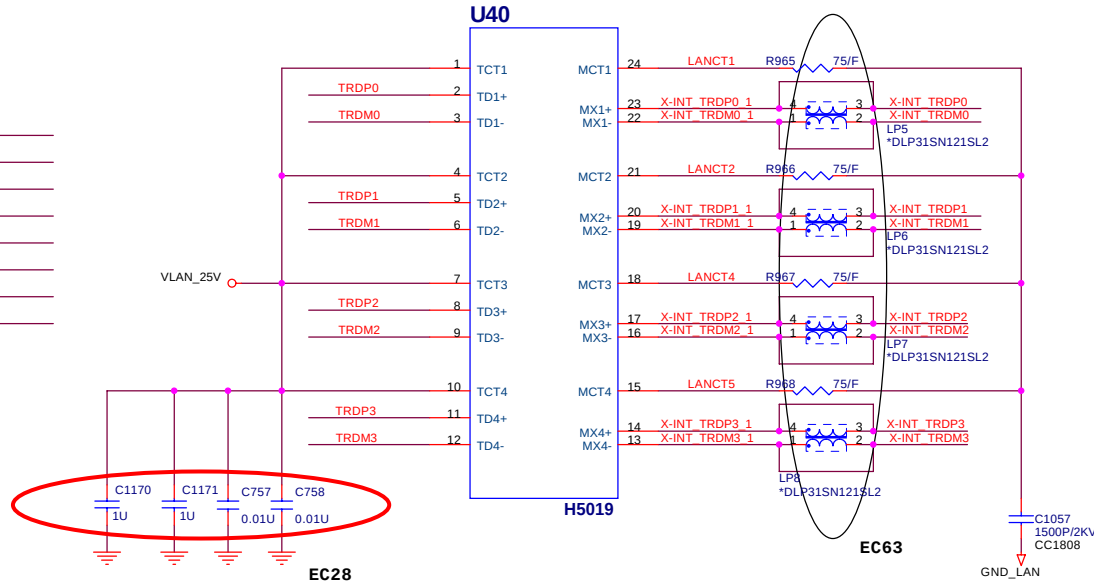
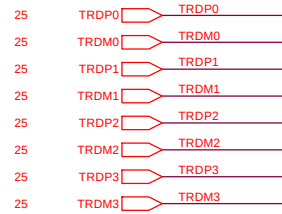
BCM4401- -10/100
BCM5788- -10/100/GIGA

25

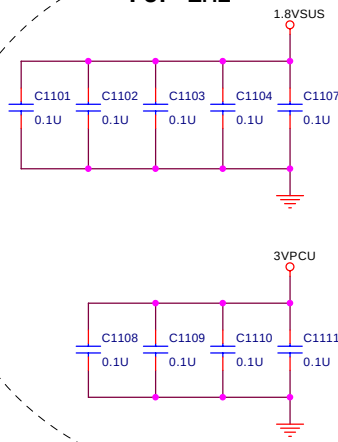


QUANTA
COMPUTER

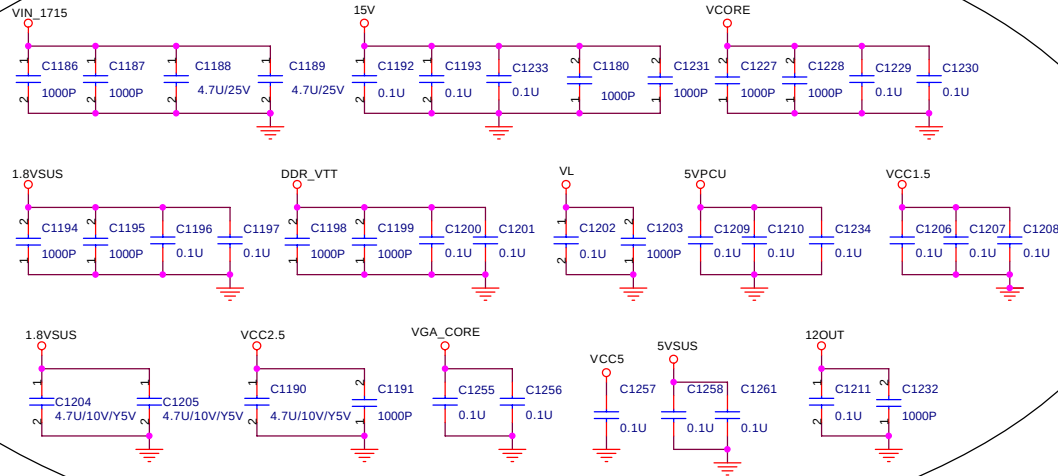
Title			
BUM5788-10/100/1G			
Size	Document Number	Rev	
A3	AW1 M/B	1B	
Date:	Wednesday, August 11, 2004	Sheet	25 of 42



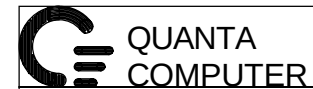
For EMI



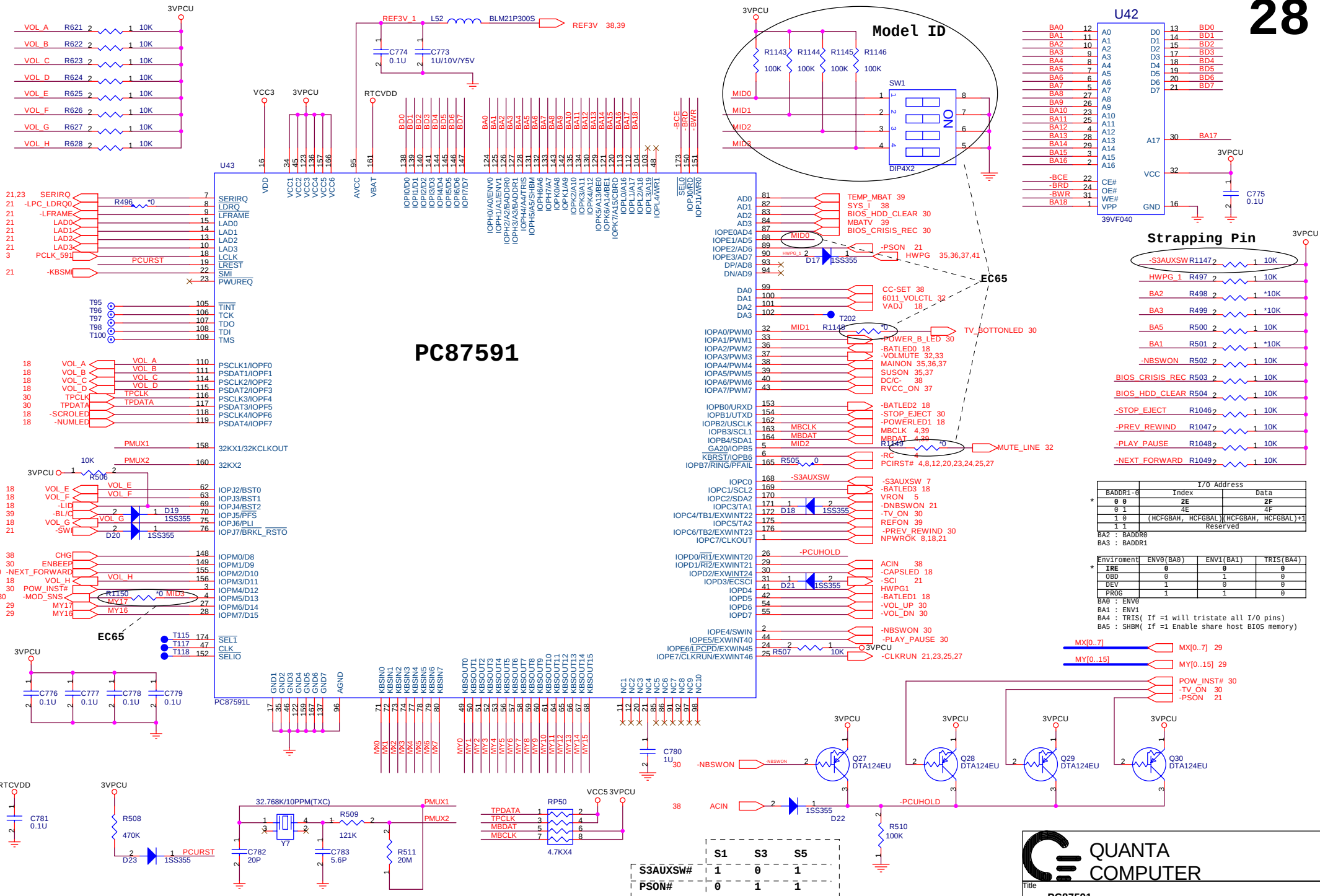
EC9



EC56



Title		
LAN(TR&CONNECTOR)		
Size	Document Number	Rev
A3	AW1 M/B	1B
Date:	Wednesday, August 11, 2004	Sheet 26 of 42



I/O Address	
BADDR1-0	Index Data
0 0	2E 2F
0 1	4E 4F
1 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1 1	Reserved

Environment	ENV0(BA0)	ENV1(BA1)	TRIS(BA4)
IRE	0	1	0
OBD	0	0	0
DEV	1	0	0
PROG	1	1	0

BA0 : ENV0
BA1 : ENV1
BA4 : TRIS(If =1 will tristate all I/O pins)
BA5 : SHBM(If =1 Enable share host BIOS memory)

QUANTA
COMPUTER

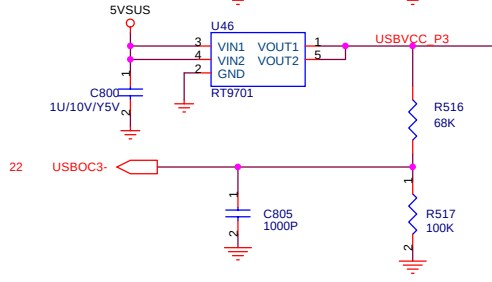
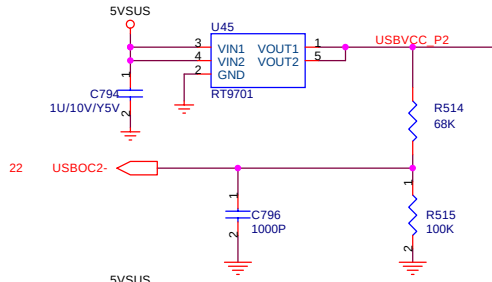
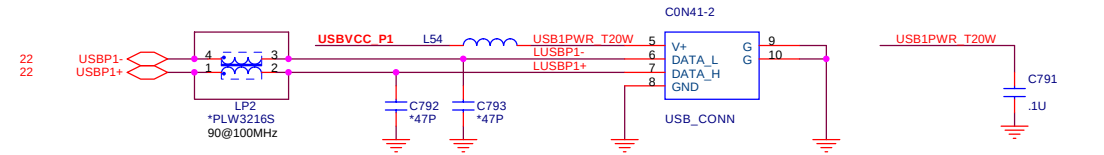
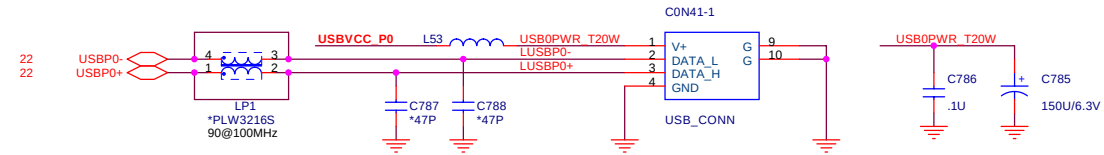
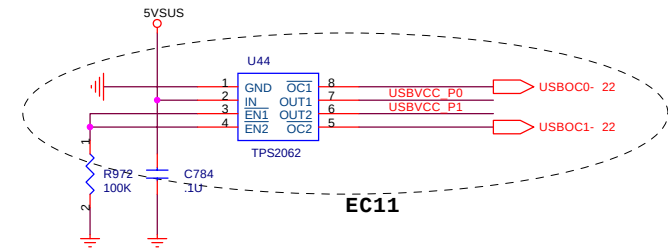
File: PC87591			
Size: A3	Document Number: AW1 M/B	Rev: 1B	
Date: Wednesday, August 11, 2004	Sheet: 28	of 42	

USB Power and Over current

USB Connector

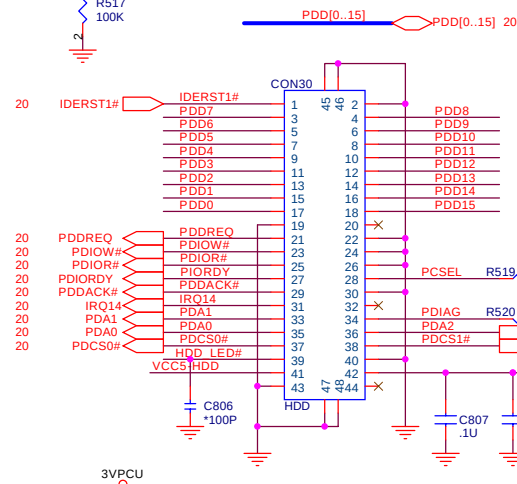
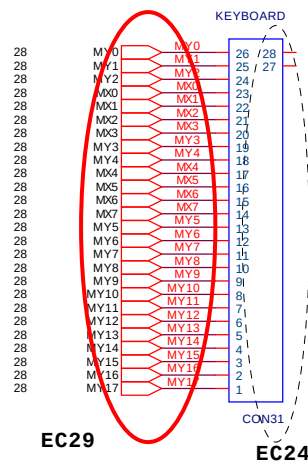
Place near the
USB connector

29

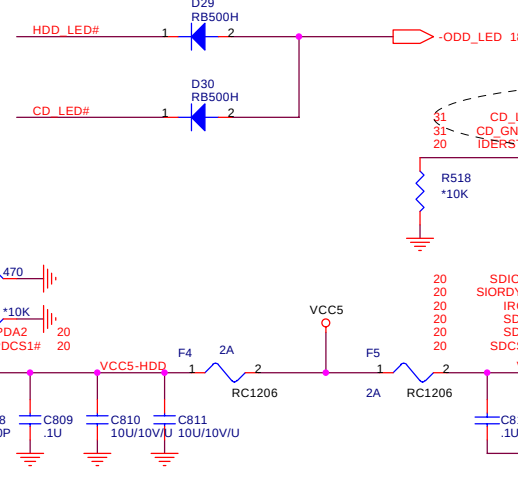
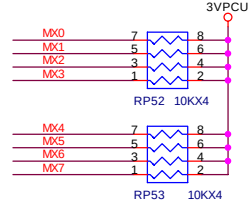


CD-ROM CONNECTOR

KEYBOARD



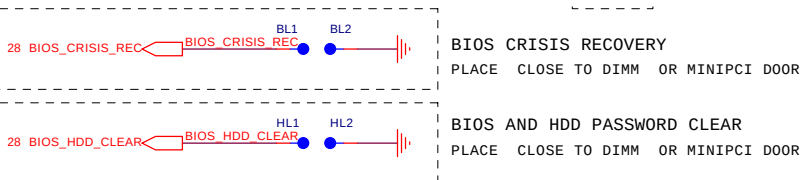
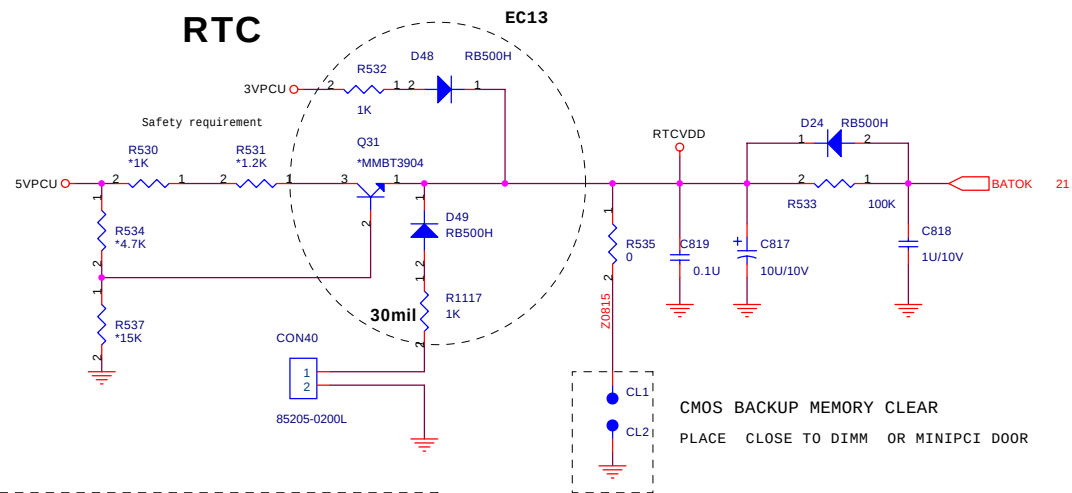
HDD CONNECTOR



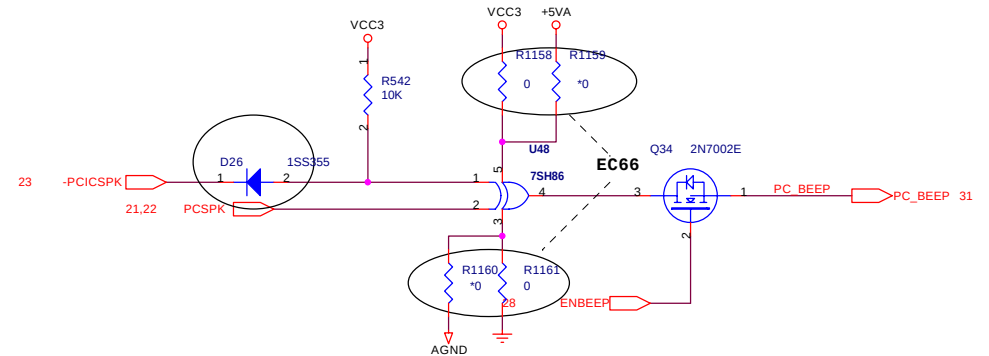
QUANTA
COMPUTER

Title			KB/USB/HDD/CDROM	
Size			Document Number	
A3			AW1 M/B	
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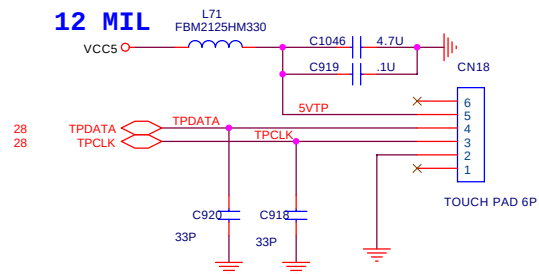
RTC



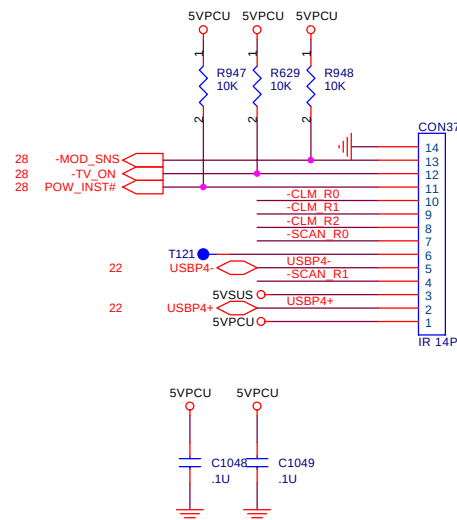
PC-BEEP



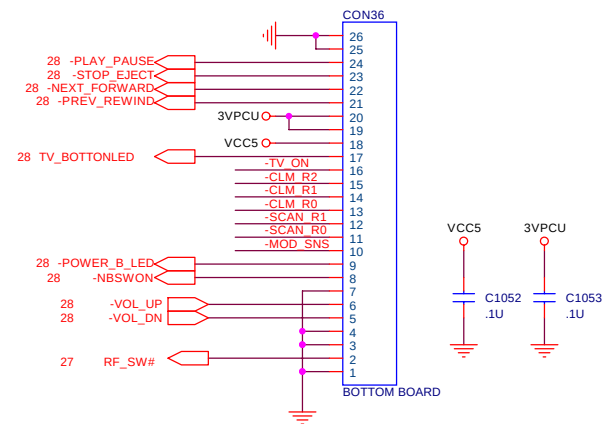
TOUCH PAD



TO RECEIVER MODULE

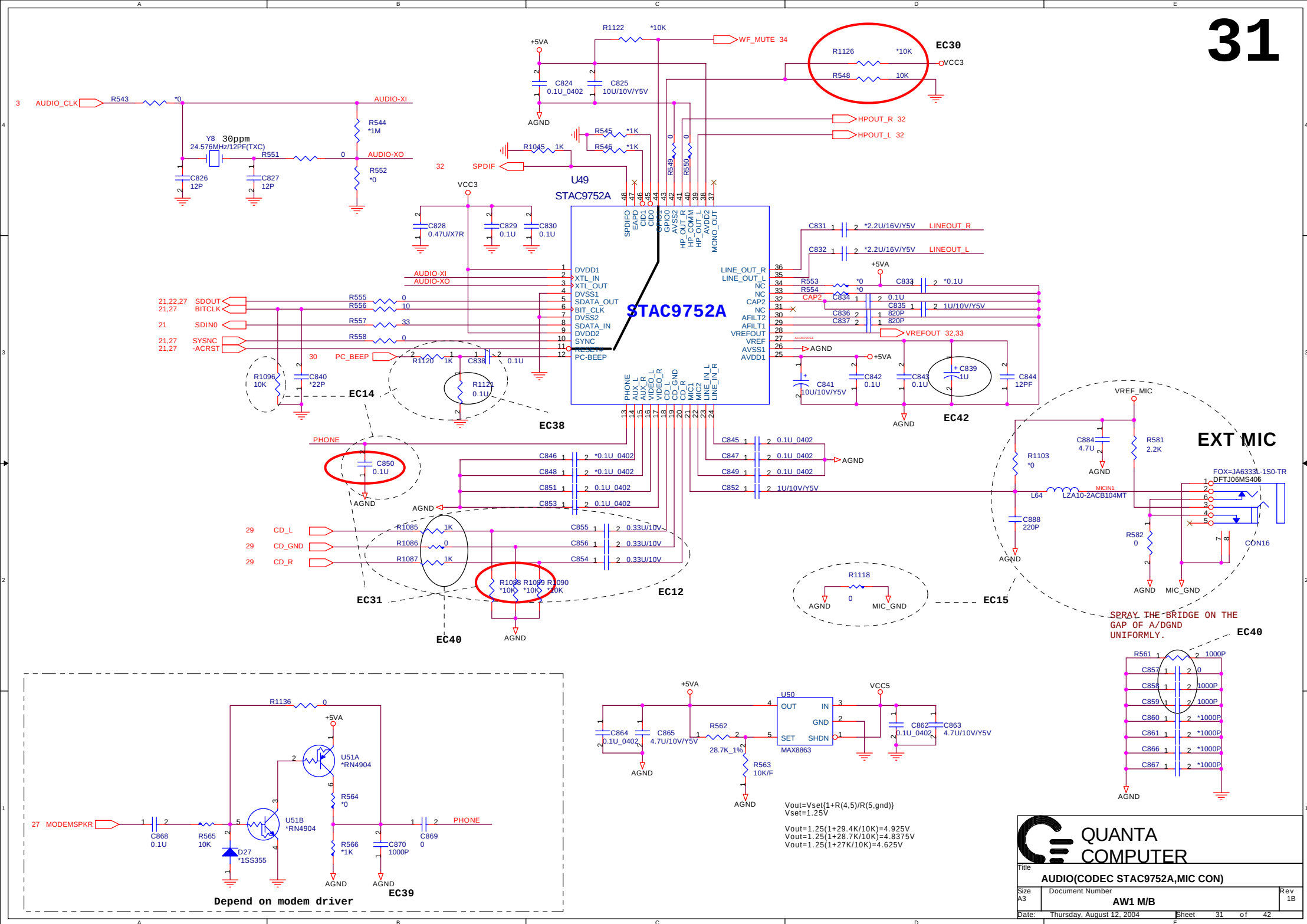


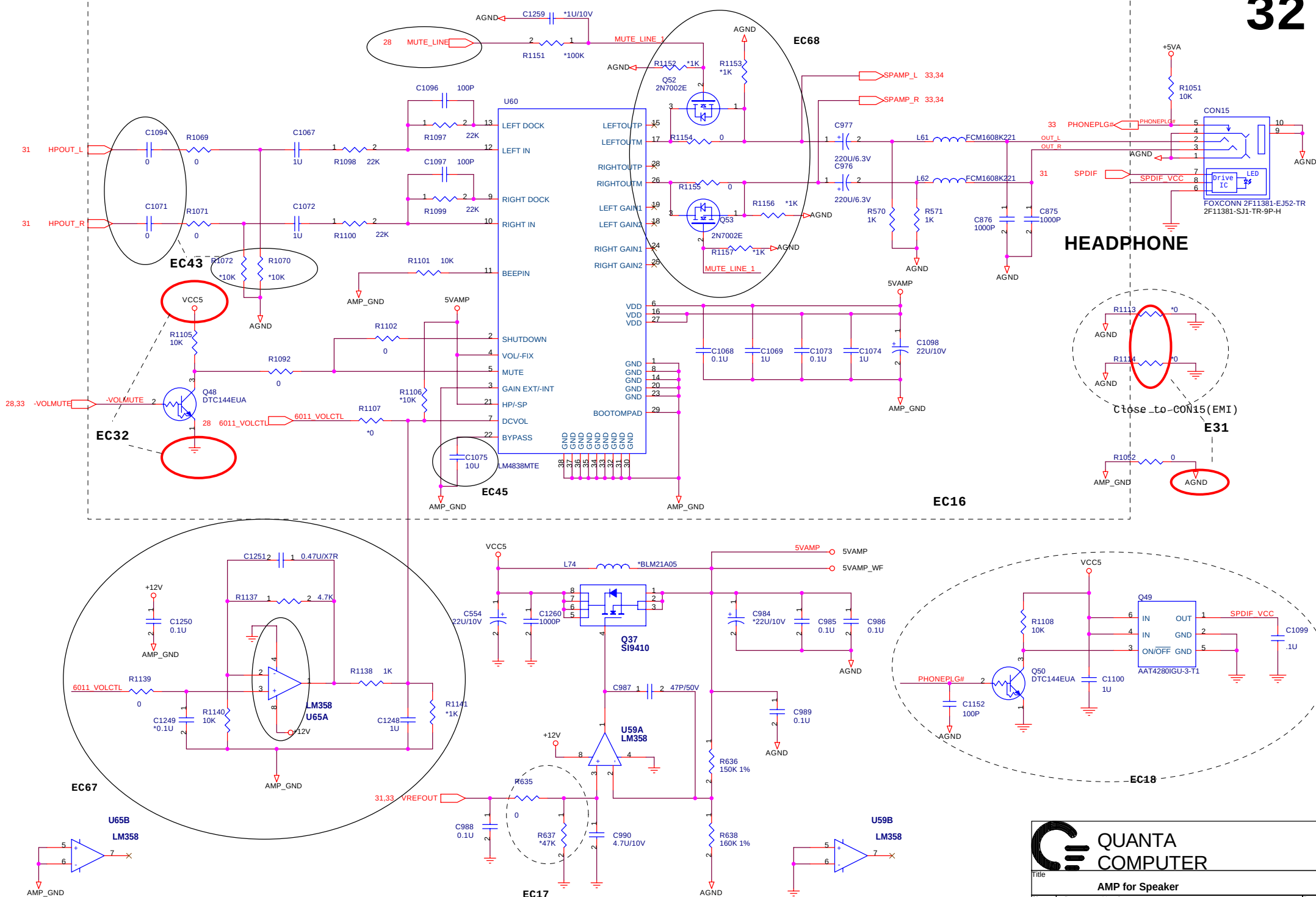
BUTTON BOARD



QUANTA
COMPUTER

Title		
FAN/RTC/PCBEEP		
Size	Document Number	Rev
A3	AW1 M/B	1B
Date:	Wednesday, August 11, 2004	Sheet 30 of 42





QUANTA
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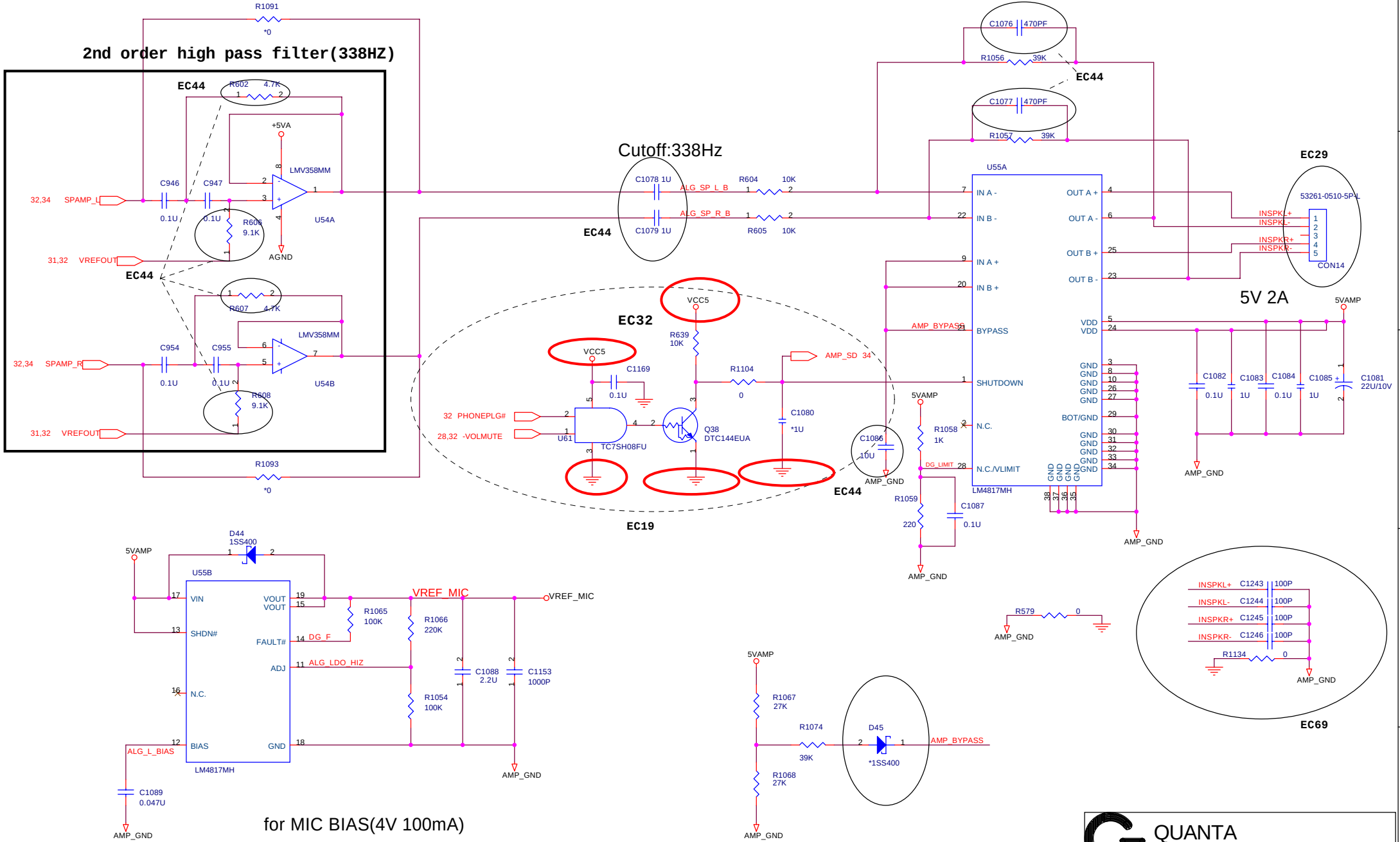
Title
AMP for Speaker

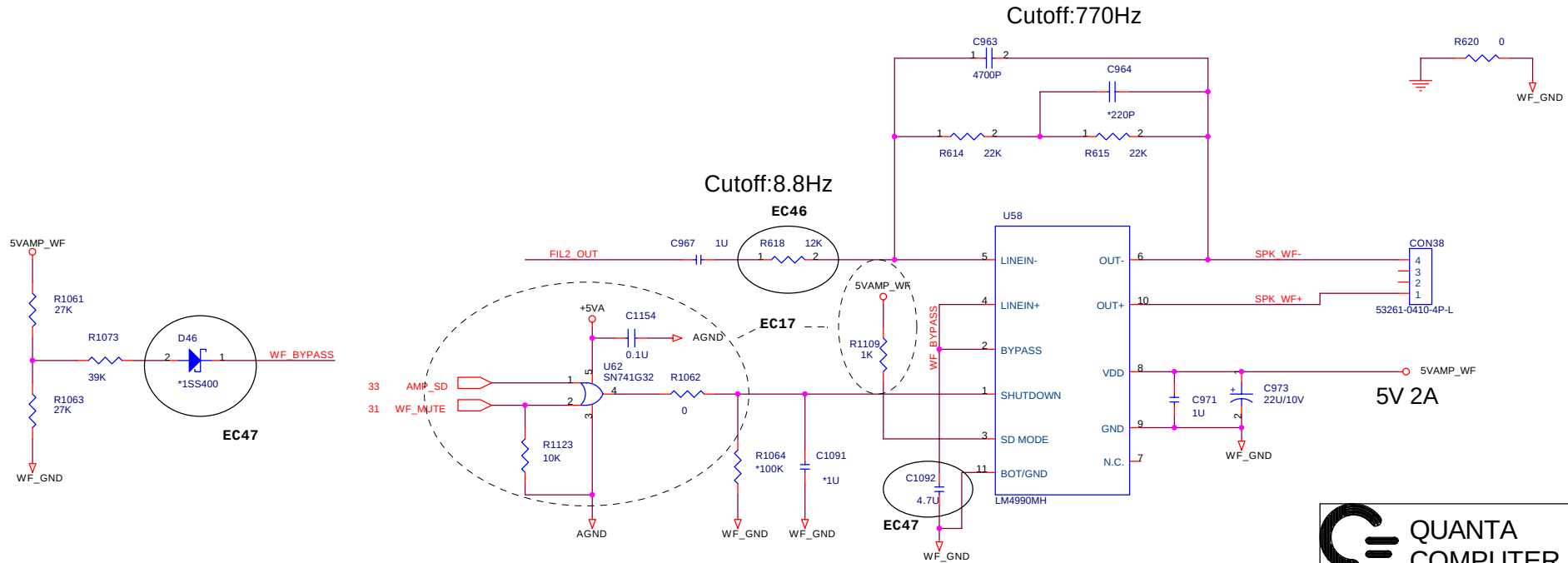
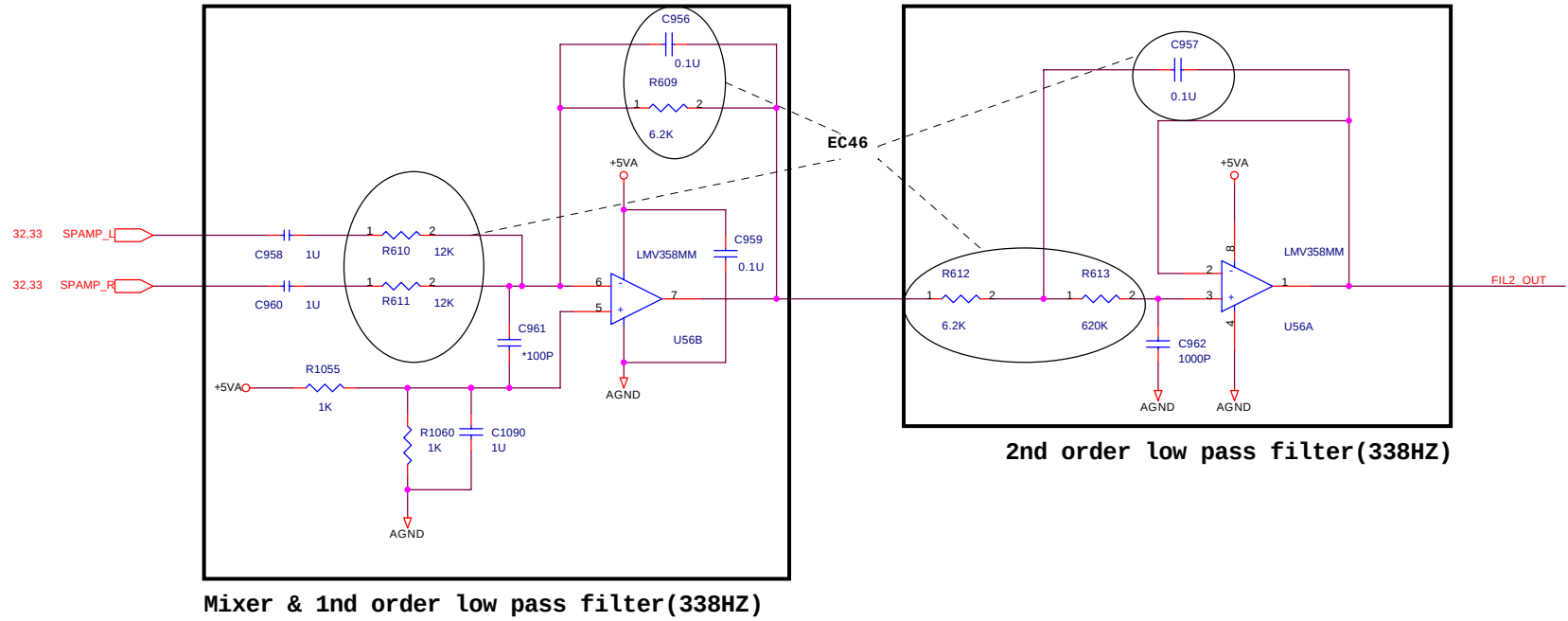
Size A3 Document Number
AW1 M/B

Date: Wednesday, August 11, 2004

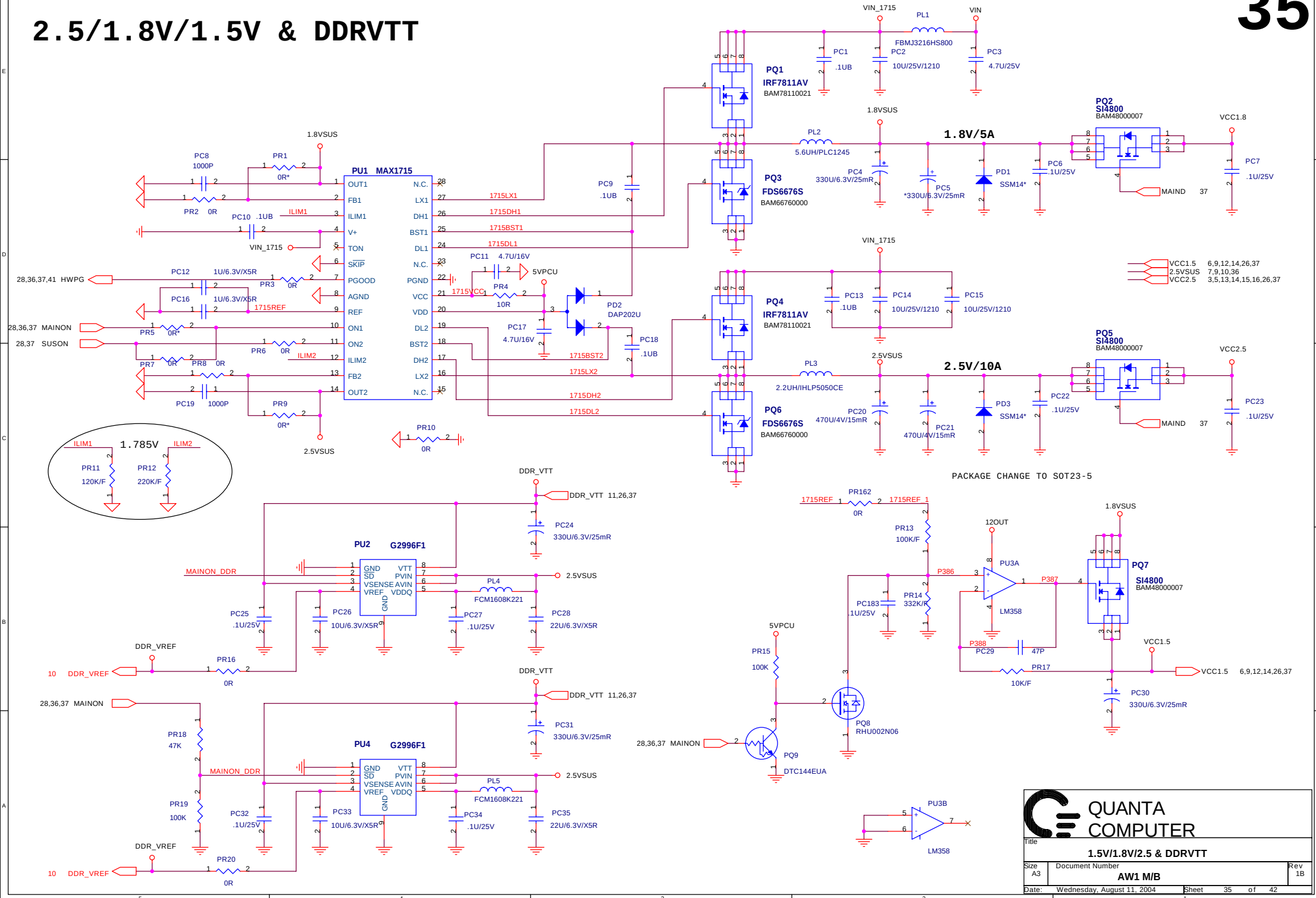
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Rev 1B





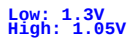
2.5/1.8V/1.5V & DDRVTT



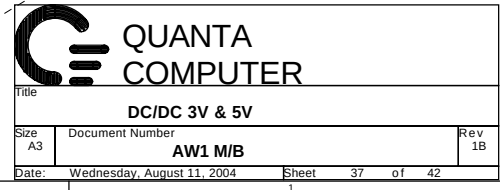
**QUANTA
COMPUTER**

Title		
1.5V/1.8V/2.5 & DDRVTT		
Size	Document Number	Rev
A3	AW1 M/B	1B
Date:	Wednesday, August 11, 2004	Sheet 35 of 42

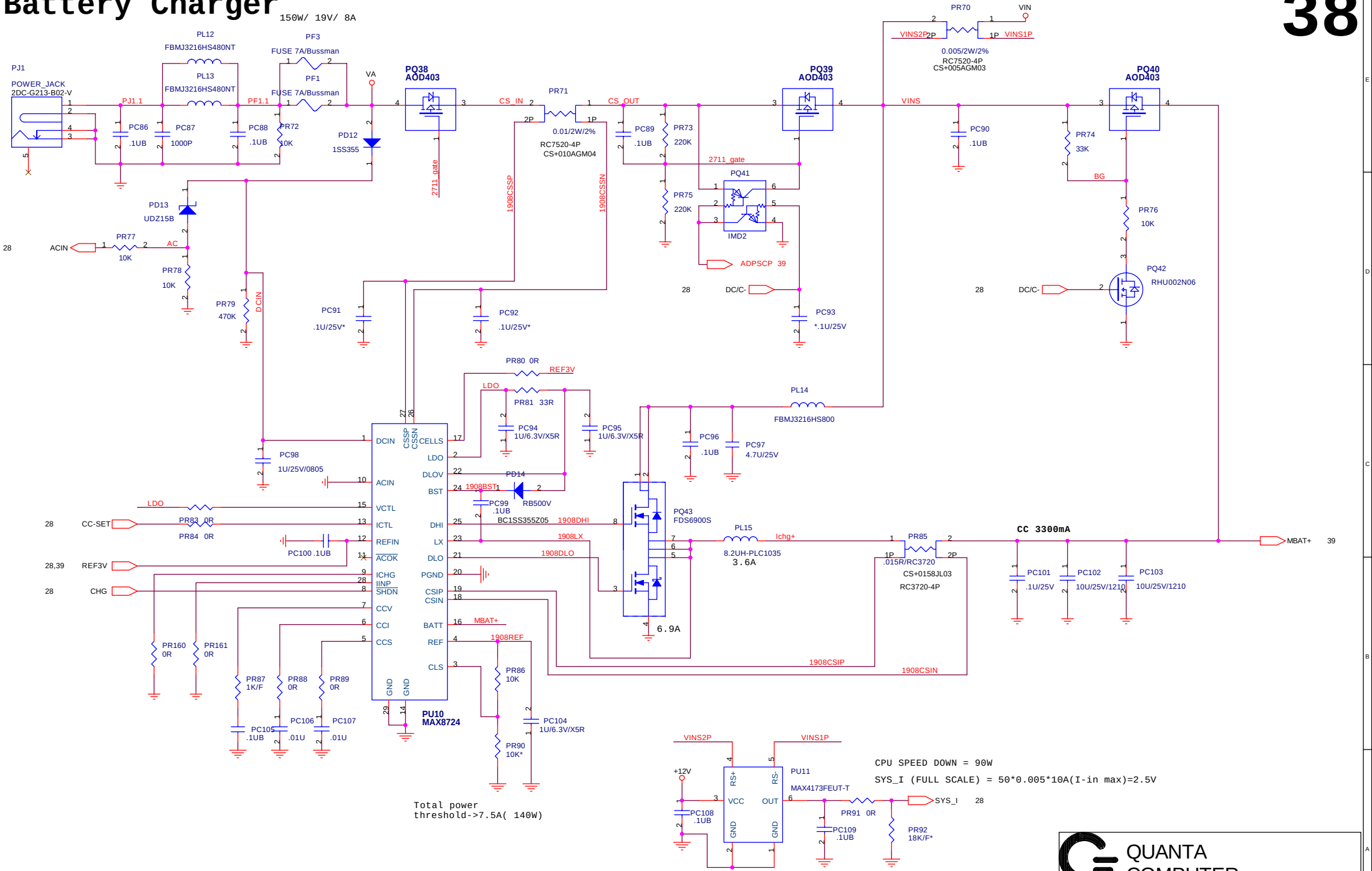
36



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Battery Charger



Total power threshold->7.5A(140W)

Only PWRON will enable this CKT.

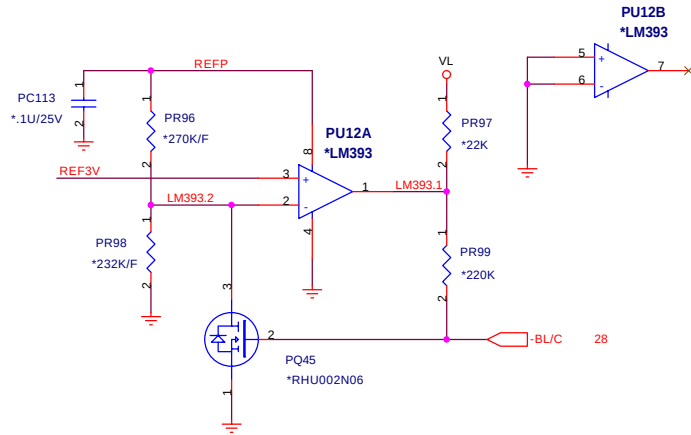


QUANTA
COMPUTER

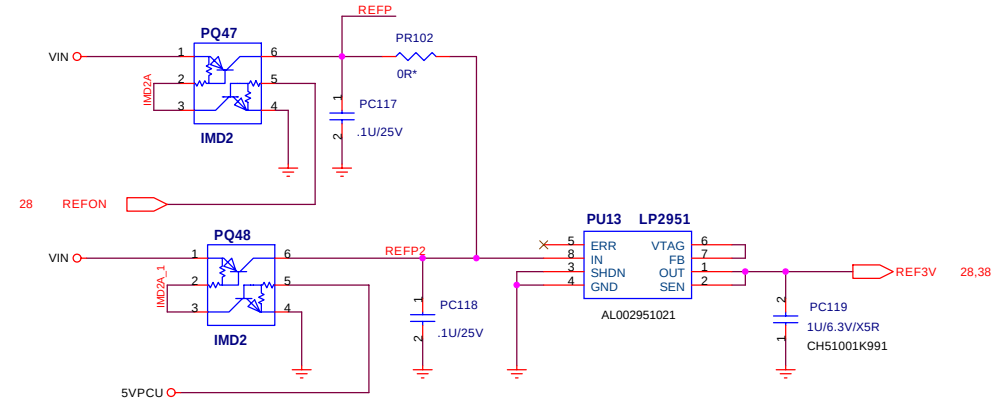
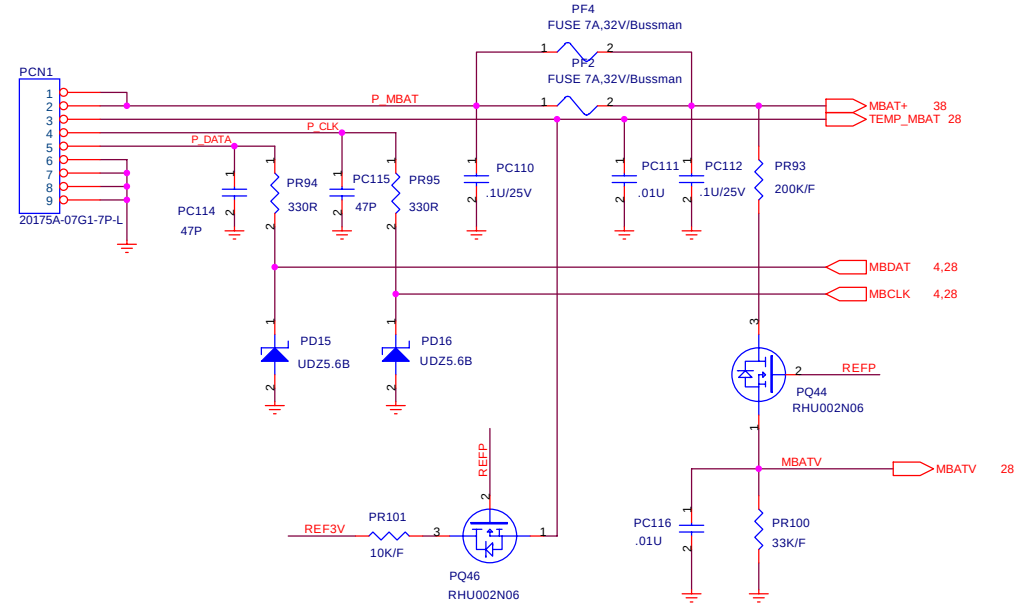
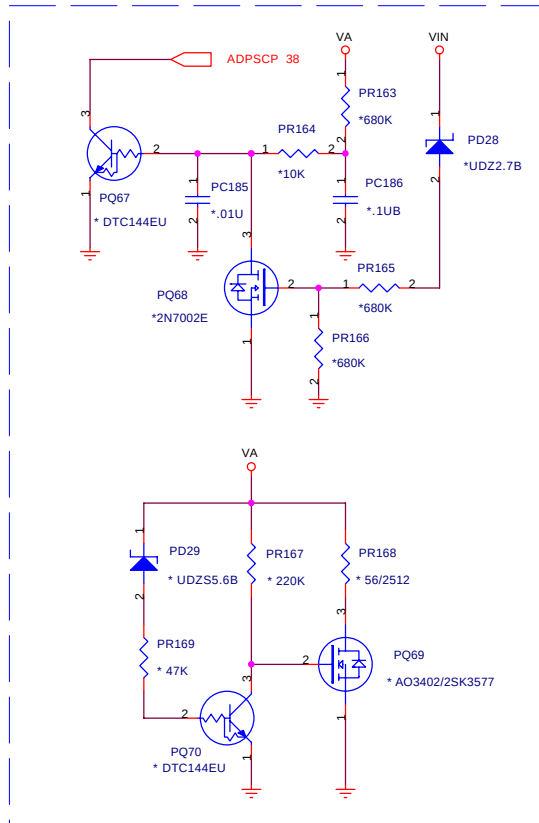
Title BATTERY CHARGER		
Size A3	Document Number AW1 M/B	Rev 1B
Date: Wednesday, August 11, 2004		Sheet 38 of 42

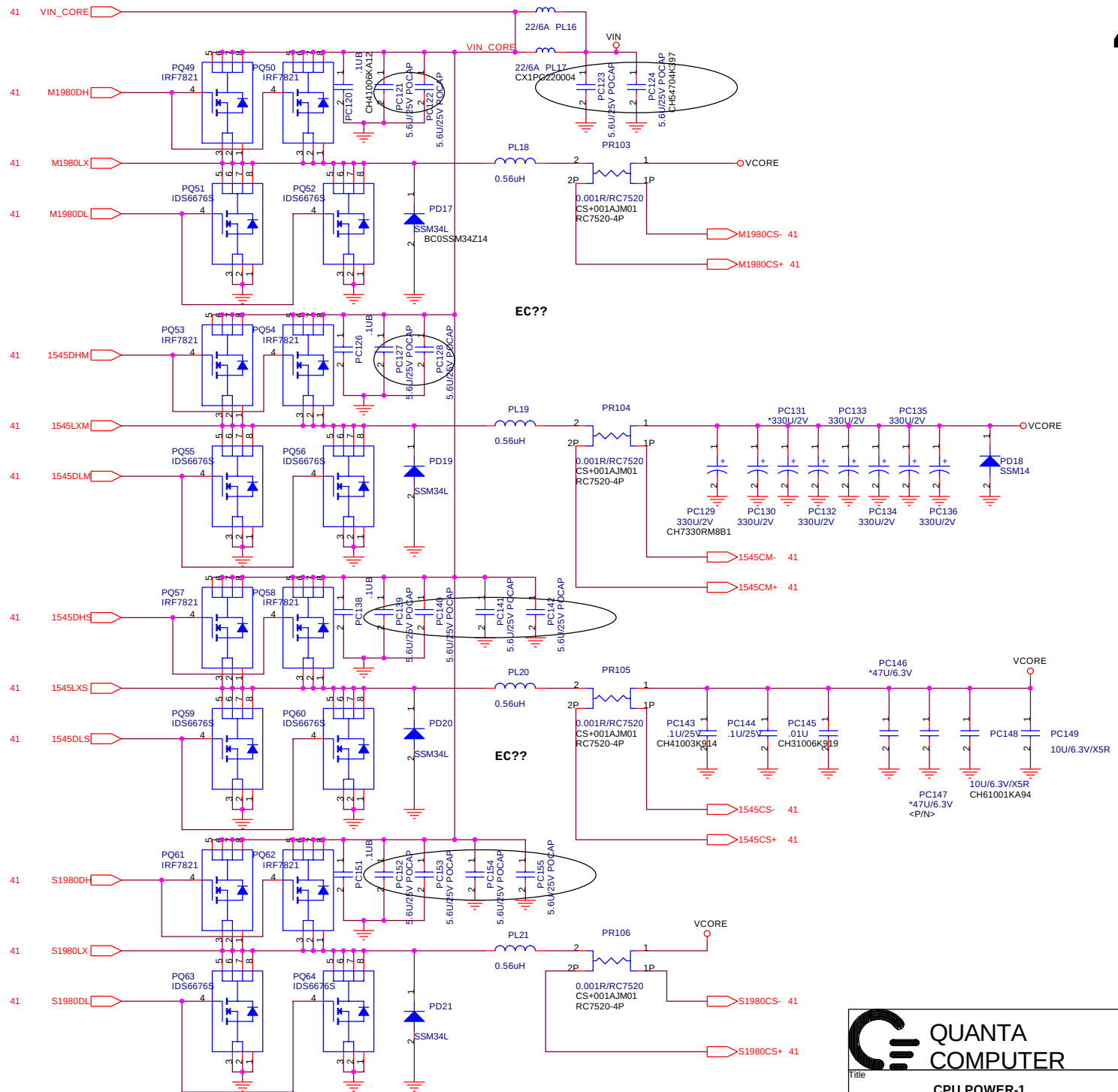
CPU SPEED DOWN = 90W
SYS_I (FULL SCALE) = 50*0.005*10A(I-in max)=2.5V

Battery Connector



SCP CKT





THIS PART SHOULD NOT CONTAIN ANY SUBSTANCES WHICH ARE SPECIFIED IN SS-00259-1.



QUANTA

COMPUTER

Title

CPU POWER-1

Size	Document Number	Rev
Custm	AW1 M/B	1B

Date:

Wednesday, August 11, 2004

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